11-/14-Bit, 5.6 GSPS, RF Digital-to-Analog Converter

Preliminary Technical Data

AD9119/AD9129

FEATURES

DAC Update Rate of up to 5.6 GSPS
Direct RF Synthesis @ 2.8 GSPS Data Rate
- **DC-to-1.4 GHz in Baseband Mode**
- **DC-to-1.0 GHz in 2x Interpolation Mode**
- **1.4 to 4.2 GHz in Mix-Mode™**

Bypassable 2x Interpolation
Excellent Dynamic performance
Supports DOCSIS 3.0 wideband ACLR/Harmonic Performance
- **8 QAM carriers: ACLR>69 dBc**

Industry Leading Single/Multicarrier IF or RF Synthesis
- **Four Carrier WCDMA ACLR @ 2457.6 MSPS**
  - **f_{OUT} = 900 MHz, ACLR=71 (Baseband mode)**
  - **f_{OUT} = 2100 MHz, ACLR=70 (Mix-Mode)**
  - **f_{OUT} = 2700 MHz, ACLR=67 (Mix-Mode)**

Dual-port LVDS and DHSTL data interface
- **Up to 1.4 GSPS Operation**
- **Source Synchronous DDR clocking with Parity Bit**

Low power: 1.1 W @ 2.8 GSPS (1.3 W @ 5.6 GSPS)

APPLICATIONS

Broadband communications systems
- **CMTS/VOD**
- **Wireless Infrastructure: WCDMA, LTE, Point-to-Point**

Instrumentation, automatic test equipment
Radar, Jammers

GENERAL DESCRIPTION

The AD9119/AD9129 are high performance 11-bit and 14-bit RF DACs supporting data rates up to 2.8 GSPS. The DAC core is based on a quad-switch architecture that enables dual-edge clocking operation effectively increasing the DAC update rate to 5.6 GSPS when configured for mix-mode or 2x interpolation. Its high dynamic range and bandwidth enables multicarrier generation up to 4.2 GHz.

In baseband mode, its wide bandwidth capability combined with high dynamic range allows it to support from 1 to 158 contiguous carriers for CATV infrastructure applications. A choice of two optional 2x interpolation filters is available to simplify the post reconstruction filter by effectively increasing the DAC update rate by a factor of two. In Mix-mode™ operation, the AD9119/AD9129 can reconstruct RF carriers in the 2nd and 3rd Nyquist zone while still maintaining exceptional dynamic range up to 4.2 GHz. Its high performance NMOS DAC core features a quad-switch architecture that enables industry-leading direct RF synthesis performance with minimal loss in output power. The output current can be programmed over a range of 9.5 mA to 34.4 mA.

The AD9119/AD9129 includes several features that may further simplify system integration. A dual-port, source synchronous LVDS interface simplifies the data interface to a host FPGA/ASIC. A differential Frame/Parity bit is also included to monitor the integrity of the interface. On-chip delay locked loops (DLLs) are used to optimize timing between different clock domains.

A serial peripheral interface (SPI) is used to configure the AD9119/AD9129 and monitor the status of readback registers. The AD9119/AD9129 is manufactured on a 0.18 µm CMOS process and operates from 1.8 V and -1.5 V supplies. It is supplied in a 160-ball chip scale ball grid array.

FUNCTIONAL BLOCK DIAGRAM

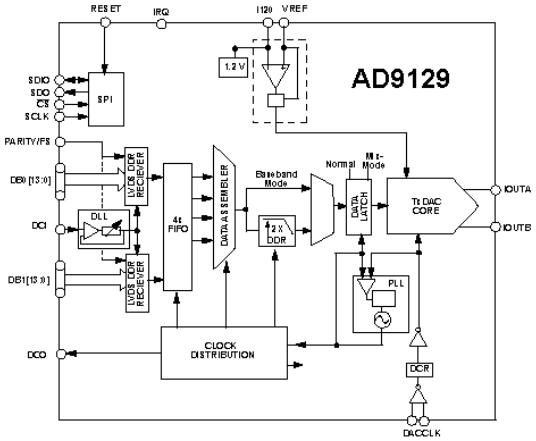


Figure 1.Product Highlights

1. High dynamic range and signal reconstruction bandwidth supports RF signal synthesis up to 4.2 GHz.
2. A dual-port interface with double data rate (DDR) LVDS data receivers supports the maximum conversion rate of 2800 MSPS.
3. Manufactured on a CMOS process, the AD9119/AD9129 uses a proprietary switching technique that enhances dynamic performance.

Pr E 11 Oct 2012

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

SPECIFICATIONS

DC SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = -1.5 V, I_{FS} = 33 mA.

Table 1.

	AD9119			AD9129			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		11			14		Bits
ACCURACY							
Integral Nonlinearity (INL)		TBD			TBD		LSB
Differential Nonlinearity (DNL)		TBD			TBD		LSB
ANALOG OUTPUTS							
Gain Error (with Internal Reference)		TBD			TBD		%
Full-Scale Output Current	9.5		34.4	9.5		34.4	mA
Output Compliance Range	1.5		2.5	1.5		2.5	V
Common Mode Output Resistance		TBD			TBD		MΩ
Differential Output Resistance		TBD			TBD		kΩ
Output Capacitance		TBD			TBD		pF
DAC CLOCK INPUT (DACCLK_P, DACCLK_N)							
Differential Peak-to-Peak Voltage	0.4	1	2	0.4	1	2	V
Common-Mode Voltage		1.2			1.2		V
TEMPERATURE DRIFT							
Gain		60			60		ppm/°C
Reference Voltage		20			20		ppm/°C
REFERENCE							
Internal Reference Voltage		1.0			1.0		V
Output Resistance		5			5		kΩ
ANALOG SUPPLY VOLTAGES							
VDDA	1.70	1.80	1.90	1.70	1.80	1.90	V
VSSA	-1.4	-1.5	-1.6	-1.4	-1.5	-1.6	
DIGITAL SUPPLY VOLTAGES							
VDD	1.70	1.8	1.90	1.70	1.8	1.90	V
SUPPLY CURRENTS AND POWER DISSIPATION 2.3 GSPS (Normal mode)							
I_{VDDA}		150			150		mA
I_{VSSA}		60			60		mA
I_{DVDD}		275			275		mA
Power Dissipation: Normal mode		1.1			1.1		W
With FIR25 enabled		1.25			1.25		W
With FIR40 enabled		1.5			1.5		W
Reduced Power Mode (Power-Down enabled: reg 0x01 = 0xEF)							
I_{VDDA}							mA
I_{VSSA}							mA
I_{VDD}							mA
SUPPLY CURRENTS AND POWER DISSIPATION 2.8 GSPS (Normal mode)							
I_{VDDA}		175			175		mA
I_{VSSA}		60			60		mA
I_{DVDD}		330			330		mA
Power Dissipation: Normal mode		1.16			1.16		W

LVDS DIGITAL SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = -1.5 V, I_{FS} = 33 mA. LVDS drivers and receivers are compliant to the IEEE Std 1596.3-1996, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
LVDS DATA INPUTS (DB0[13:0]P, DB0[13:0]N, DB1[13:0]P, DB1[13:0]N) DB+ = V_{IA}, DB−= V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}	825		1575	mV
Input Differential Threshold, V_{IDTH}	−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$		20		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
LVDS Input Rate		1400		MSPS
LVDS Minimum Data Valid Period (t_{MDE}) Refer to figure xxx			??	ps
Input Capacitance		1.2		pF
LVDS CLOCK INPUT (DCI_P, DCI_N) DCI_P = V_{IA}, DCI_N = V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}	825		1575	mV
Input Differential Threshold, V_{IDTH}	−200		+200	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$		20		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Maximum Clock Rate		700		MHz
LVDS CLOCK OUTPUT (DCO_P, DCO_N) DCO_P = V_{OA}, DCO_N = V_{OB} 100 Ω Termination				
Output Voltage High, V_{OA} or V_{OB}			1375	mV
Output Voltage Low, V_{OA} or V_{OB}	1025			mV
Output Differential Voltage, $\|V_{OD}\|$	150	200	250	mV
Output Offset Voltage, V_{OS}	1150		1250	mV
Output Impedance, Single-Ended, R_O	80	100	120	Ω
R_O Mismatch Between A and B, ΔRO			10	%
Change in $\|V_{OD}\|$ Between 0 and 1, $\|\Delta V_{OD}\|$			25	mV
Change in V_{OS} Between 0 and 1, ΔV_{OS}			25	mV
Output Current, Driver Shorted to Ground, I_{SA}, I_{SB}			20	mA
Output Current, Drivers Shorted Together, I_{SAB}			4	mA
Power-Off Output Leakage, $\|I_{XA}\|$, $\|I_{XB}\|$			10	mA
Maximum Clock Rate		700		MHz

HSTL DIGITAL SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = -1.5 V, I_{FS} = 33 mA. HSTL receiver levels are compliant to the JEDEC JESD8-6 standard, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
HSTL DATA INPUTS				
(DB0[13:0]P, DB0[13:0]N, DB1[13:0]P, DB1[13:0]N) DB+ = V_{IA}, DB−= V_{IB}				
Common Mode Input Voltage Range, V_{IA} or V_{IB}	0.68		0.9	V
Differential Input Voltage	TBD	300	TBD	mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
HSTL Input Rate		1400		MSPS
HSTL Minimum Data Valid Period (t_{MDE}) Refer to figure xxx			??	ps
Input Capacitance		1.2		pF
HSTL CLOCK INPUT				
(DCI_P, DCI_N) DCI_P = V_{IA}, DCI_N = V_{IB}				
Common Mode Input Voltage Range, V_{IA} or V_{IB}	TBD		TBD	mV
Differential Input Voltage	TBD		TBD	mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Maximum Clock Rate		700		MHz

SERIAL PORT AND CMOS PIN SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = -1.5 V, I_{FS} = 33 mA.

Table 4.

Parameter	Min	Typ	Max	Unit
WRITE OPERATION (see Figure 75xxxx)				
SCLK Clock Rate (f_{SCLK}, $1/t_{SCLK}$)			20	MHz
SCLK Clock High, (t_{HI})	20			ns
SCLK Clock Low, (t_{LOW})	20			ns
SDIO to SCLK Setup Time, (t_{DS})	10			ns
SCLK to SDIO Hold Time, (t_{DH})	5			ns
$\overline{CS}$ to SCLK Setup Time, (t_S)	10			ns
SCLK to $\overline{CS}$ Hold Time, (t_H)	5			ns
READ OPERATION (see Figure xxxx76 and xxxx77)				
SCLK Clock Rate (f_{SCLK}, $1/t_{SCLK}$)			20	MHz
SCLK Clock High, (t_{HI})	20			ns
SCLK Clock Low, (t_{LOW})	20			ns
SDIO to SCLK Setup Time, (t_{DS})	10			ns
SCLK to SDIO Hold Time, (t_{DH})	5			ns
$\overline{CS}$ to SCLK Setup Time, (t_S)	10			ns
SCLK to SDIO (or SDO) Data Valid Time, (t_{DV})			10	ns
$\overline{CS}$ to SDIO (or SDO) Output Valid to Hi-Z, (t_{EZ})		2		
INPUTS (SDI, SDIO, SCLK, $\overline{CS}$)				
Voltage in High, V_{IH}	1.1	1.8		V
Voltage in Low, V_{IL}		0	0.4	V
Current in High, I_{IH}	−10		+10	µA
Current in Low, I_{IL}	−10		+10	µA
OUTPUT (SDIO, SYNC)				
Voltage Out High, V_{OH}	1.3		2.0	V
Voltage Out Low, V_{OL}	0		0.2	V

Parameter	Min	Typ	Max	Unit
Current Out High, I_{OH}		4		mA
Current Out Low, I_{OL}		4		mA

AC SPECIFICATIONS

VDDA = VDD = 1.8 V, VSSA = -1.5 V, I_{FS} = 33 mA.

Table 5.

	AD9119			AD9129			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE							
DAC Update Rate (DACCLK Input)	1400		2800	1400		2800	MSPS
Adjusted DAC Update Rate[1]	1400		2800	1400		2800	
Output Settling Time to 0.1%		13			13		nsec
SPURIOUS-FREE DYNAMIC RANGE (SFDR)							
f_{DAC} = 2400 MSPS							
f_{OUT} = 100 MHz		TBD			TBD		dBc
f_{OUT} = 350 MHz		TBD			TBD		dBc
f_{OUT} = 550 MHz		TBD			TBD		dBc
f_{OUT} = 950 MHz		TBD			TBD		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)							
f_{DAC} = 2400 MSPS $f_{OUT2} = f_{OUT1} + 1.4$ MHz							
f_{OUT} = 100 MHz		TBD			TBD		dBc
f_{OUT} = 350 MHz		TBD			TBD		dBc
f_{OUT} = 550 MHz		TBD			TBD		dBc
f_{OUT} = 950 MHz		TBD			TBD		dBc

Parameter	AD9119 Min	AD9119 Typ	AD9119 Max	AD9129 Min	AD9129 Typ	AD9129 Max	Unit
NOISE SPECTRAL DENSITY (NSD)							
Single Tone, f_{DAC} = 2400 MSPS							
f_{OUT} = 100 MHz		TBD			TBD		dBm/Hz
f_{OUT} = 350MHz		TBD			TBD		dBm/Hz
f_{OUT} = 550 MHz		TBD			TBD		dBm/Hz
f_{OUT} = 850 MHz		TBD			TBD		dBm/Hz
Target DOCSIS ACLR Performance (50-1000MHz) at 6+MHz offset							
8 Contiguous Carriers		69			69		
16 Contiguous Carriers		66			66		
32 Contiguous Carriers		63			63		
Target WCDMA ACLR (Single Carrier)							
Adjacent Channel							
f_{DAC} = 2457.6 MSPS f_{OUT} = 350 MHz		80			80		dBc
f_{DAC}= 2457.6 MSPS, f_{OUT} = 950 MHz		78			78		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1700 MHz (Mix-Mode)		73.5			73.5		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2100 MHz (Mix-Mode)		69			69		dBc
Target Alternate Adjacent Channel							
f_{DAC} = 2457.6 MSPS, f_{OUT} = 350 MHz		80			80		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 950 MHz		79			79		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1700 MHz (Mix-Mode)		74			74		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2100 MHz (Mix-Mode)		72			72		dBc

[1] Adjusted DAC update rate is calculated as f_{DAC} divided by the minimum required interpolation factor. For the AD9119/AD9129, the minimum interpolation factor is 1. Thus, with f_{DAC} = 2800 MSPS, f_{DAC} adjusted = 2800 MSPS.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	With Respect To	Rating
DCI, DCO	VSS	−0.3 V to VDD + 0.3 V
LVDS Data Inputs	VSS	−0.3 V to VDD + 0.3 V
IOUTP, IOUTN	VSSA	VSSA – 0.3V to +2.5V
I250U, VREF	VSSA	VSSA −0.3 V to VDDA + 0.3 V
IRQ, $\overline{CS}$, SCLK, SDO, SDIO, RESET, SYNC	VSS	−0.3 V to VDD + 0.3 V
Junction Temperature		150°C
Operating Temperature		-40°C to +85°C
Storage Temperature		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
160-Ball CSP_BGA	31.2	7.0	°C/W[1]

[1] With no airflow movement.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 8. AD9119 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	I250U	Nominal 1.0 V Reference. Tie to VSSA via a 4.0 kΩ resistor to generate a 250 µA reference current.
A2	VREF	Voltage Reference Input/Output. Decouple to VSSA with 1 nF capacitor.
A3, A4, B3, B4, B5, C4, C5, C6	VSSA	-1.5V Analog Supply Voltage Input.
A5, A8, B6, B7	VDDA Shield	+1.8V Analog Supply Shield. Tie to VDDA at the DAC.
A9, A10, A11, B1, B2, B8, B9, B10, B11, C2, C3, C7, C8, C9, C10, D2, D3, D4, D7, E1, E2	VDDA	+1.8V Analog Supply Voltage Input.
G12, G13, G14, H11, H12, H13, H14, J3, J4, J11, J12, J13, J14	VDD	+1.8V Digital Supply Voltage Input.
C13, C14, D12, D13, D14, E11, E12, E13, E14, F11, F12, F13, F14, G1, G2, G3, G11, H3, H4	VSS	+1.8V Digital Supply Return.
A12, A13, A14, B12, B13, C11, C12, D5, D6, D8, D9, D10, D11, E3, E4, F1, F2, F3, F4, G4	VSSC	Analog Supply Return.
A6	IP	DAC's Positive Current Output Source.
A7	IN	DAC's Negative Current Output Source.
B14	SYNC	Synchronization signal output
C1, D1	CLKN, CLKP	Negative/Positive DAC Clock Input (DACCLK).
H1	RESET	RESET input. Active HIGH. Tie to VSS if unused.
H2	IRQ	Interrupt Request Open Drain Output. Active HIGH. Pull up to VDD with a 1 kΩ resistor.
J1	SDIO	Serial Port Data Input/Output
J2	SDO	Serial Port Data Output
K1	SCLK	Serial Port Clock Input
K2	$\overline{CS}$	Serial Port Enable Input
K3, K4	DCI_P, DCI_N	Positive, Negative Data Clock Input (DCI)
K11, K12	DCO_P/DCO_N	Positive, Negative Data Clock Output (DCO).
K13, K14	FRM_P, FRM_N	Positive, Negative Data Frame/Parity signal (FRAME/PARITY)
L1, M1	NC, NC	Do not connect to this pin
L2, M2	NC, NC	Do not connect to this pin
L3, M3	NC, NC	Do not connect to this pin
L4, M4	P1_D0P, P1_D0N	Port 1 Positive/Negative Data Input Bit 0.
L5, M5	P1_D1P, P1_D1N	Port 1 Positive/Negative Data Input Bit 1.
L6, M6	P1_D2P, P1_D2N	Port 1 Positive/Negative Data Input Bit 2.
L7, M7	P1_D3P, P1_D3N	Port 1 Positive/Negative Data Input Bit 3.
L8, M8	P1_D4P, P1_D4N	Port 1 Positive/Negative Data Input Bit 4.
L9, M9	P1_D5P, P1_D5N	Port 1 Positive/Negative Data Input Bit 5.
L10, M10	P1_D6P, P1_D6N	Port 1 Positive/Negative Data Input Bit 6.
L11, M11	P1_D7P, P1_D7N	Port 1 Positive/Negative Data Input Bit 7.
L12,M12	P1_D8P, P1_D8N	Port 1 Positive/Negative Data Input Bit 8.
L13, M13	P1_D9P, P1_D9N	Port 1 Positive/Negative Data Input Bit 9.
L14, M14	P1_D10P, P1_D10N	Port 1 Positive/Negative Data Input Bit 10.
N1, P1	NC, NC	Do not connect to this pin
N2, P2	NC, NC	Do not connect to this pin

Pin No.	Mnemonic	Description
N3, P3	NC, NC	Do not connect to this pin
N4, P4	P0_D0P, P0_D0N	Port 0 Positive/Negative Data Input Bit 0.
N5, P5	P0_D1P, P0_D1N	Port 0 Positive/Negative Data Input Bit 1.
N6, P6	P0_D2P, P0_D2N	Port 0 Positive/Negative Data Input Bit 2.
N7, P7	P0_D3P, P0_D3N	Port 0 Positive/Negative Data Input Bit 3.
N8, P8	P0_D4P, P0_D4N	Port 0 Positive/Negative Data Input Bit 4.
N9, P9	P0_D5P, P0_D5N	Port 0 Positive/Negative Data Input Bit 5.
N10, P10	P0_D6P, P0_D6N	Port 0 Positive/Negative Data Input Bit 6.
N11, P11	P0_D7P, P0_D7N	Port 0 Positive/Negative Data Input Bit 7.
N12, P12	P0_D8P, P0_D8N	Port 0 Positive/Negative Data Input Bit 8.
N13, P13	P0_D9P, P0_D9N	Port 0 Positive/Negative Data Input Bit 9.
N14, P14	P0_D10P, P0_D10N	Port 0 Positive/Negative Data Input Bit 10.

Table 9. AD9129 Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	I250U	Nominal 1.0 V Reference. Tie to VSSA via a 4.0 kΩ resistor to generate a 250 µA reference current.
A2	VREF	Voltage Reference Input/Output. Decouple to VSSA with 1 nF capacitor.
A3, A4, B3, B4, B5, C4, C5, C6	VSSA	-1.5V Analog Supply Voltage Input.
A5, A8, B6, B7	VDDA Shield	+1.8V Analog Supply Shield. Tie to VDDA at the DAC.
A9, A10, A11, B1, B2, B8, B9, B10, B11, C2, C3, C7, C8, C9, C10, D2, D3, D4, D7, E1, E2	VDDA	+1.8V Analog Supply Voltage Input.
G12, G13, G14, H11, H12, H13, H14, J3, J4, J11, J12, J13, J14	VDD	+1.8V Digital Supply Voltage Input.
C13, C14, D12, D13, D14, E11, E12, E13, E14, F11, F12, F13, F14, G1, G2, G3, G11, H3, H4	VSS	+1.8V Digital Supply Return.
A12, A13, A14, B12, B13, C11, C12, D5, D6, D8, D9, D10, D11, E3, E4, F1, F2, F3, F4, G4	VSSC	Analog Supply Return.
A6	IP	DAC's Positive Current Output Source.
A7	IN	DAC's Negative Current Output Source.
B14	SYNC	Synchronization signal output
C1, D1	CLKN, CLKP	Negative/Positive DAC Clock Input (DACCLK).
H1	RESET	RESET input. Active HIGH. Tie to VSS if unused.
H2	IRQ	Interrupt Request Open Drain Output. Active HIGH. Pull up to VDD with a 1 kΩ resistor.
J1	SDIO	Serial Port Data Input/Output
J2	SDO	Serial Port Data Output
K1	SCLK	Serial Port Clock Input
K2	$\overline{CS}$	Serial Port Enable Input
K3, K4	DCI_P, DCI_N	Positive, Negative Data Clock Input (DCI)
K11, K12	DCO_P/DCO_N	Positive, Negative Data Clock Output (DCO).
K13, K14	FRM_P, FRM_N	Positive, Negative Data Frame/Parity signal (FRAME/PARITY)
L1, M1	P1_D0P, P1_D0N	Port 1 Positive/Negative Data Input Bit 0.
L2, M2	P1_D1P, P1_D1N	Port 1 Positive/Negative Data Input Bit 1.

Pin No.	Mnemonic	Description
L3, M3	P1_D2P, P1_D2N	Port 1 Positive/Negative Data Input Bit 2.
L4, M4	P1_D3P, P1_D3N	Port 1 Positive/Negative Data Input Bit 3.
L5, M5	P1_D4P, P1_D4N	Port 1 Positive/Negative Data Input Bit 4.
L6, M6	P1_D5P, P1_D5N	Port 1 Positive/Negative Data Input Bit 5.
L7, M7	P1_D6P, P1_D6N	Port 1 Positive/Negative Data Input Bit 6.
L8, M8	P1_D7P, P1_D7N	Port 1 Positive/Negative Data Input Bit 7.
L9, M9	P1_D8P, P1_D8N	Port 1 Positive/Negative Data Input Bit 8.
L10, M10	P1_D9P, P1_D9N	Port 1 Positive/Negative Data Input Bit 9.
L11, M11	P1_D10P, P1_D10N	Port 1 Positive/Negative Data Input Bit 10.
L12,M12	P1_D11P, P1_D11N	Port 1 Positive/Negative Data Input Bit 11.
L13, M13	P1_D12P, P1_D12N	Port 1 Positive/Negative Data Input Bit 12.
L14, M14	P1_D13P, P1_D13N	Port 1 Positive/Negative Data Input Bit 13.
N1, P1	P0_D0P, P0_D0N	Port 0 Positive/Negative Data Input Bit 0.
N2, P2	P0_D1P, P0_D1N	Port 0 Positive/Negative Data Input Bit 1.
N3, P3	P0_D2P, P0_D2N	Port 0 Positive/Negative Data Input Bit 2.
N4, P4	P0_D3P, P0_D3N	Port 0 Positive/Negative Data Input Bit 3.
N5, P5	P0_D4P, P0_D4N	Port 0 Positive/Negative Data Input Bit 4.
N6, P6	P0_D5P, P0_D5N	Port 0 Positive/Negative Data Input Bit 5.
N7, P7	P0_D6P, P0_D6N	Port 0 Positive/Negative Data Input Bit 6.
N8, P8	P0_D7P, P0_D7N	Port 0 Positive/Negative Data Input Bit 7.
N9, P9	P0_D8P, P0_D8N	Port 0 Positive/Negative Data Input Bit 8.
N10, P10	P0_D9P, P0_D9N	Port 0 Positive/Negative Data Input Bit 9.
N11, P11	P0_D10P, P0_D10N	Port 0 Positive/Negative Data Input Bit 10.
N12, P12	P0_D11P, P0_D11N	Port 0 Positive/Negative Data Input Bit 11.
N13, P13	P0_D12P, P0_D12N	Port 0 Positive/Negative Data Input Bit 12.
N14, P14	P0_D13P, P0_D13N	Port 0 Positive/Negative Data Input Bit 13.

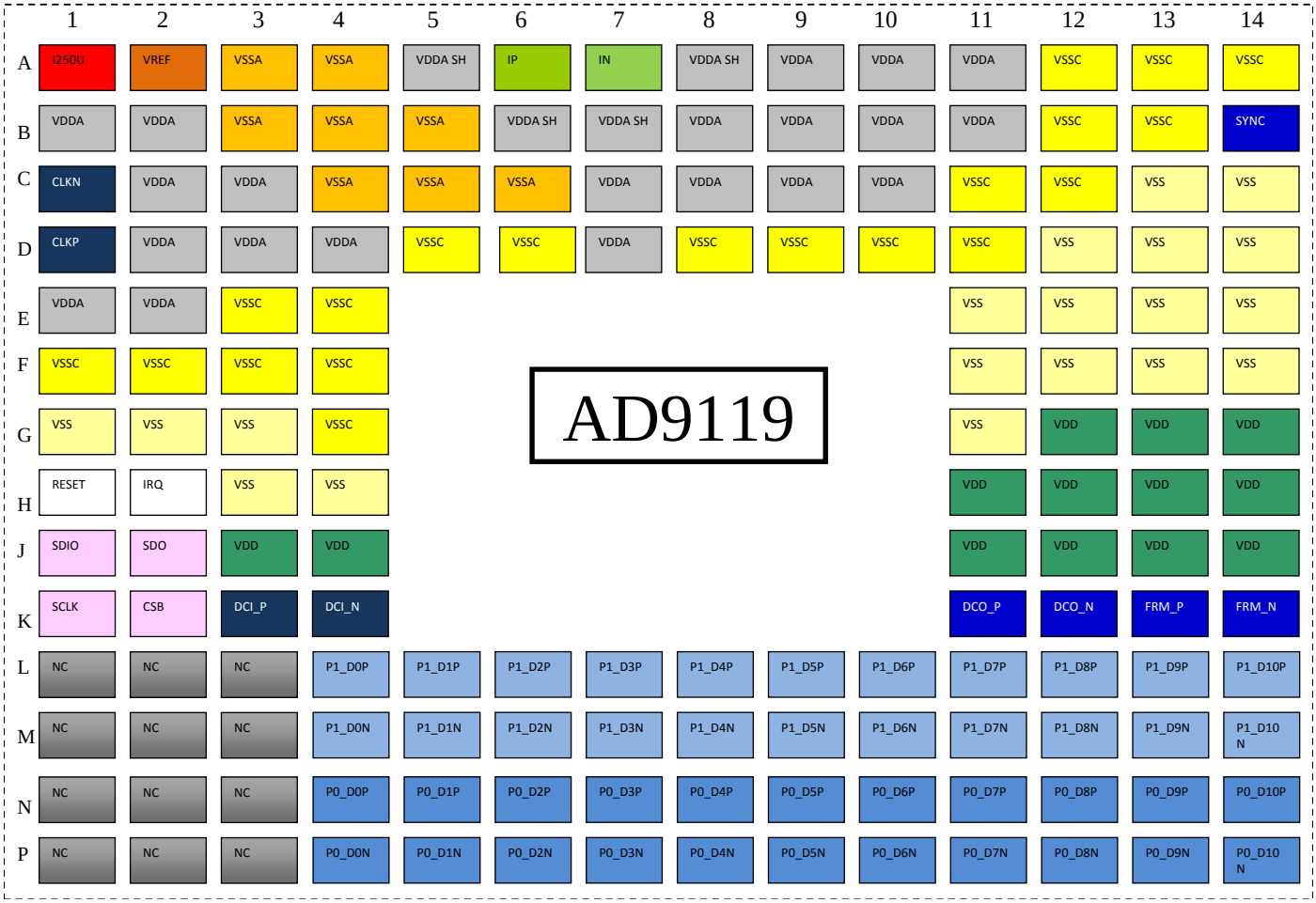


Figure 2. AD9119 Pin function diagram

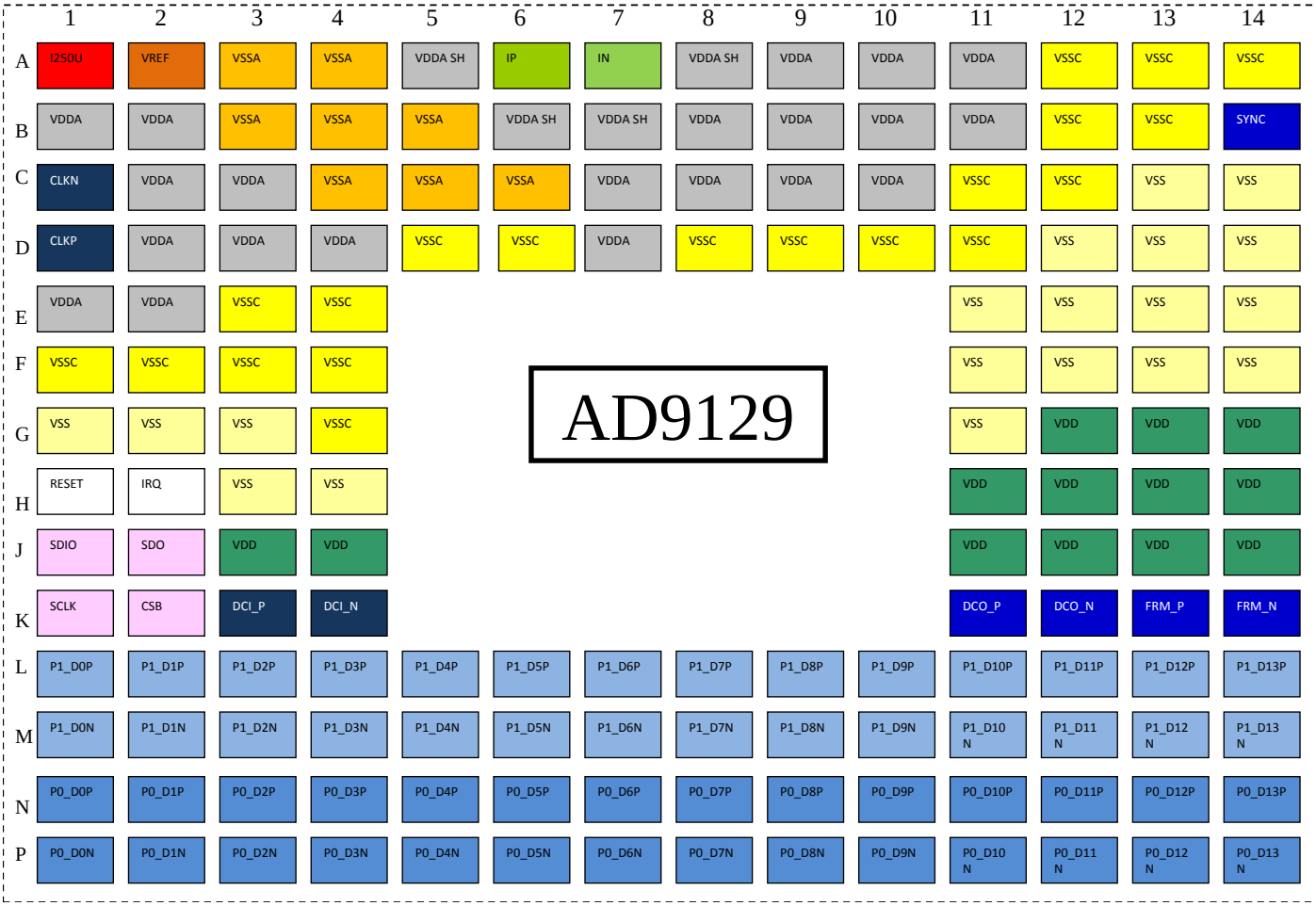


Figure 3. AD9129 Pin function diagram

TYPICAL PERFORMANCE CHARACTERISTICS – AD9119

STATIC LINEARITY

I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

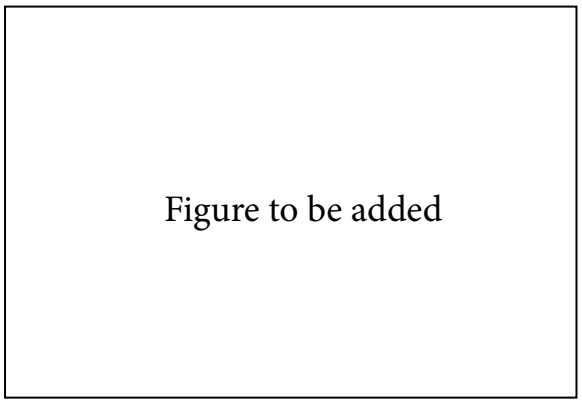


Figure 4. Typical INL, 11 mA at 25°C

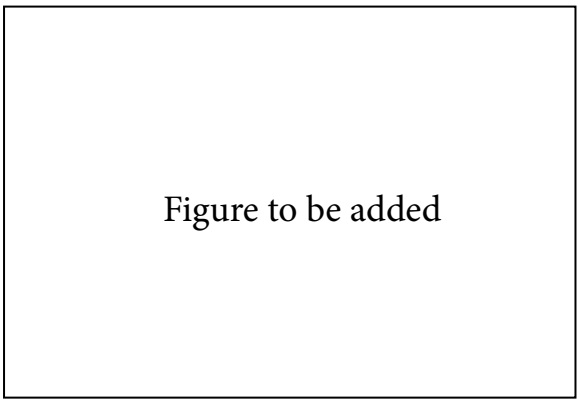


Figure 7. Typical DNL, 11 mA at 25°C

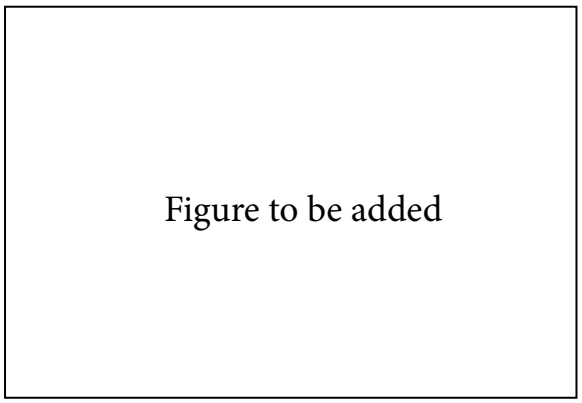


Figure 5. Typical INL, 22 mA at 25°C

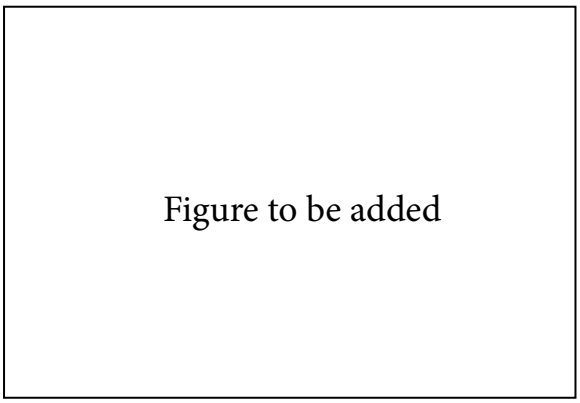


Figure 8. Typical DNL, 22 mA at 25°C

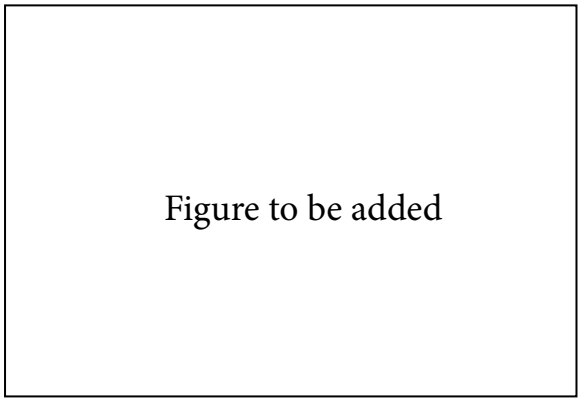


Figure 6. Typical INL, 33 mA at 25°C

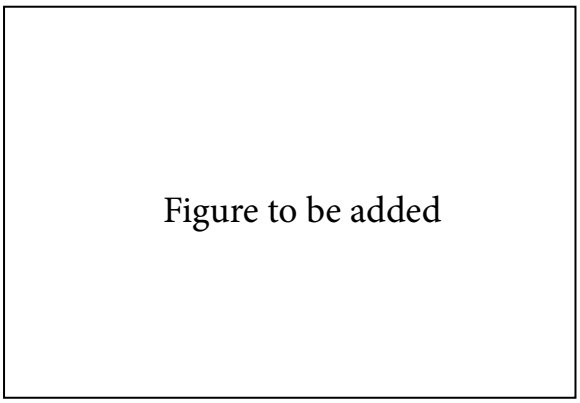


Figure 9. Typical DNL, 33 mA at 25°C

AC (NORMAL MODE)

I_{OUTFS} = 28 mA, nominal supplies, f_{DAC} = 2.6 GSPS, T_A = 25°C, unless otherwise noted.

Figure to be added

Figure 10. Single Tone Spectrum at f_{OUT} = 70 MHz

Figure to be added

Figure 11. Single-Tone Spectrum at f_{OUT} = 1000 MHz

Figure to be added

Figure 12. SFDR vs. f_{OUT} over f_{DAC}

Figure to be added

Figure 13. IMD vs. f_{OUT} over f_{DAC}

Figure to be added

Figure 14. Single-Tone NSD over f_{OUT}

Figure to be added

Figure 15. WCDMA NSD over f_{OUT}

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

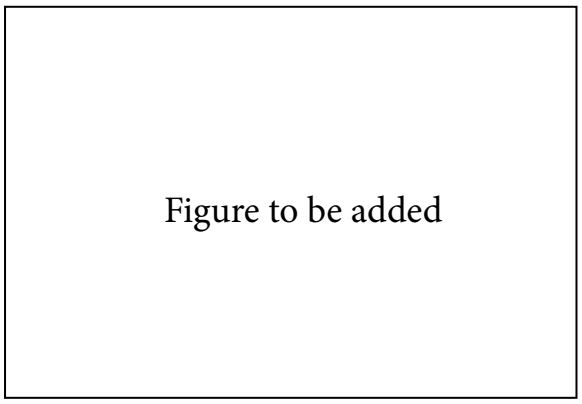


Figure 16. SFDR vs. f_{OUT} over Digital Full Scale

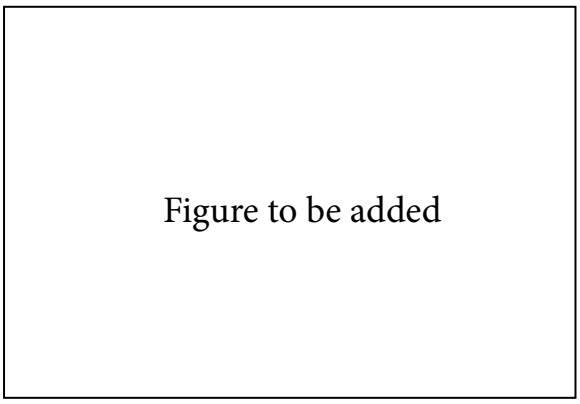


Figure 19. IMD vs. f_{OUT} over Digital Full Scale

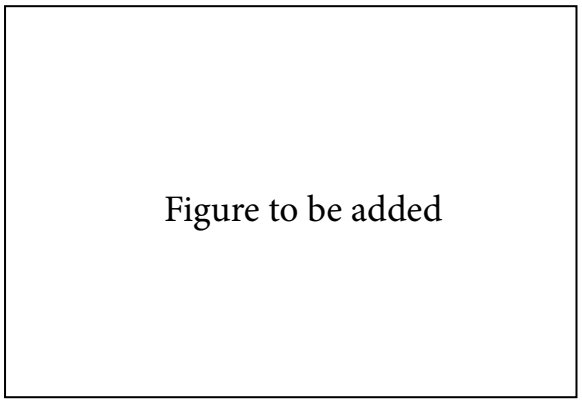


Figure 17. SFDR for Second Harmonic vs. f_{OUT} over Digital Full Scale

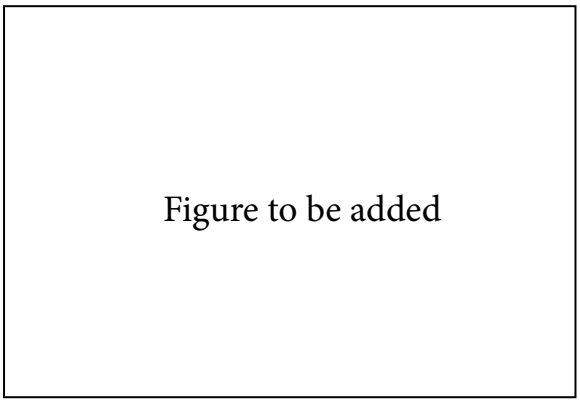


Figure 20. SFDR vs. f_{OUT} over DAC I_{OUTFS}

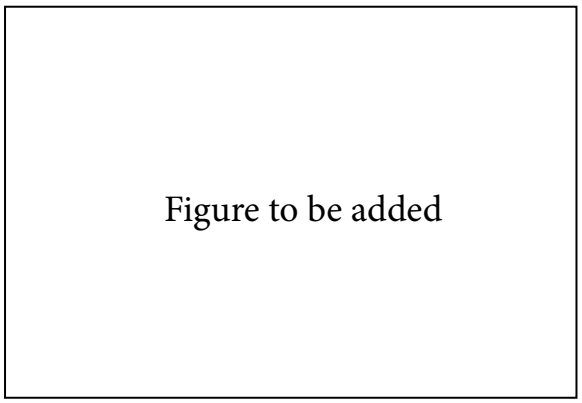


Figure 18. SFDR for Third Harmonic vs. f_{OUT} over Digital Full Scale

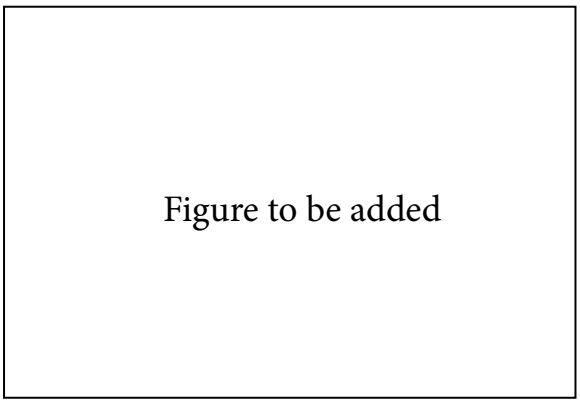


Figure 21. IMD vs. f_{OUT} over DAC I_{OUTFS}

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

Figure to be added

Figure 22. SFDR vs. f_{OUT} over Temperature

Figure to be added

Figure 23. IMD vs. f_{OUT} over Temperature

Figure to be added

Figure 24. Single Tone NSD vs. f_{OUT} over Temperature

Figure to be added

Figure 25. WCDMA NSD vs. f_{OUT} over Temperature

Figure to be added

Figure 26. Single carrier WCDMA at 877.5 MHz

Figure to be added

Figure 27. Two carrier WCDMA at 875 MHz

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

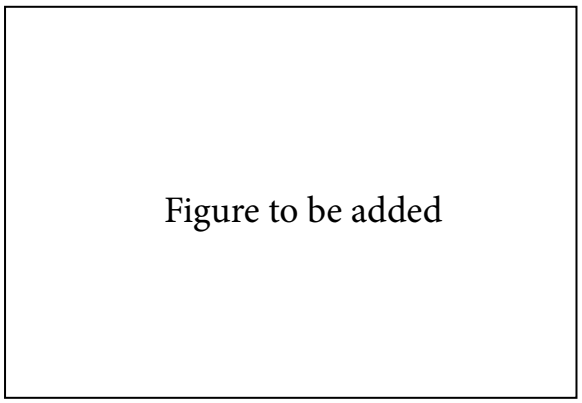


Figure 28. Single Carrier WCDMA ACLR vs. f_{OUT}

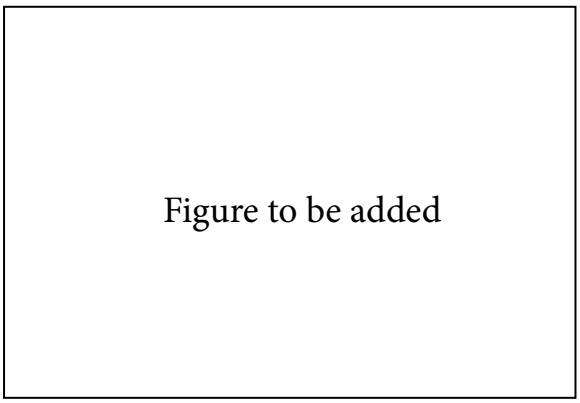


Figure 29. Two Carrier WCDMA ACLR vs. f_{OUT}

AC (MIX-MODE)

I_{OUTFS} = 28 mA, nominal supplies, f_{DAC} = 2.6 GSPS, T_A = 25°C, unless otherwise noted.

Figure to be added

Figure 30. Single Tone Spectrum at f_{OUT} = 2350 MHz

Figure to be added

Figure 31. Single-Tone Spectrum at f_{OUT} = 1600 MHz

Figure to be added

Figure 32. SFDR vs. f_{OUT} over f_{DAC}

Figure to be added

Figure 33. IMD vs. f_{OUT} over f_{DAC}

Figure to be added

Figure 34. Single-Tone NSD over f_{OUT}

Figure to be added

Figure 35. WCDMA NSD over f_{OUT}

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

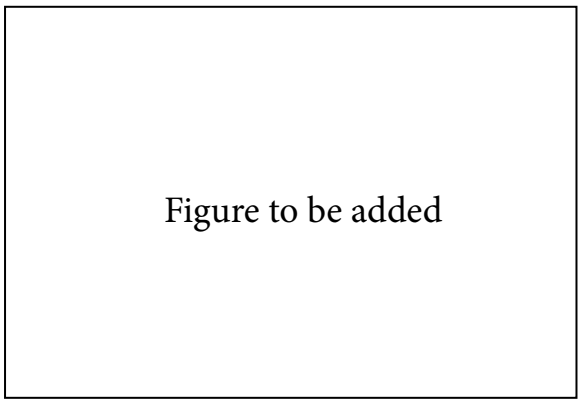


Figure 36. SFDR vs. f_{OUT} over Digital Full Scale

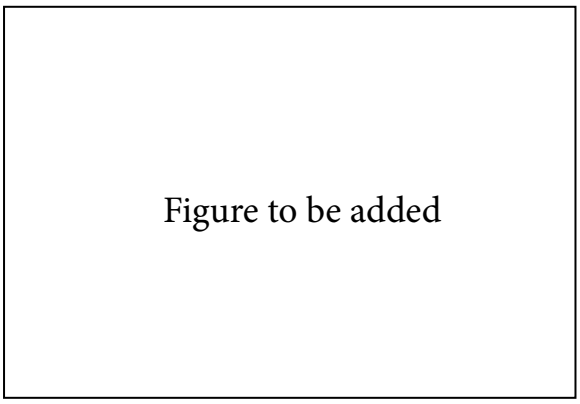


Figure 39. IMD vs. f_{OUT} over Digital Full Scale

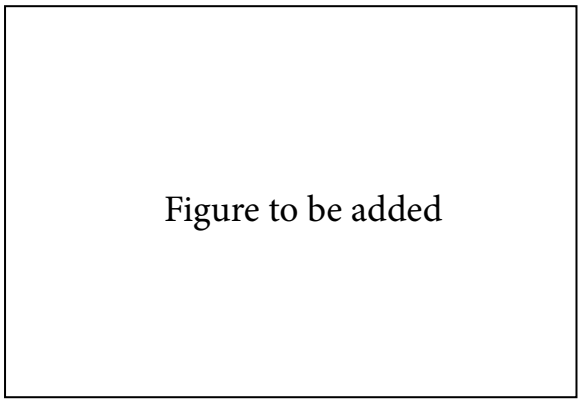


Figure 37. SFDR for Second Harmonic vs. f_{OUT} over Digital Full Scale

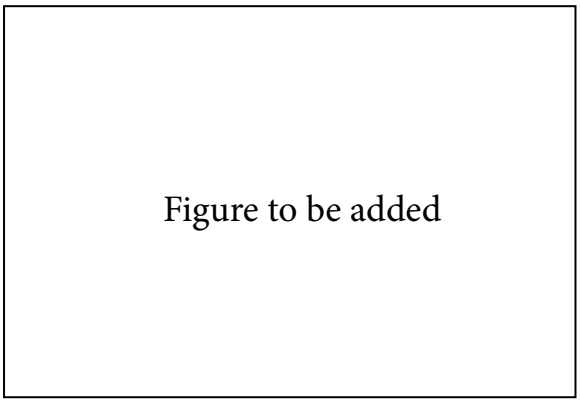


Figure 40. SFDR vs. f_{OUT} over DAC I_{OUTFS}

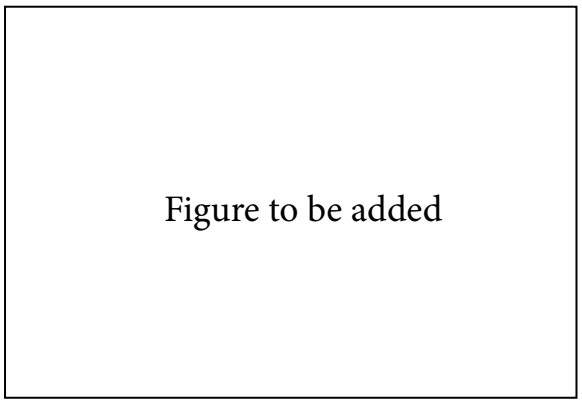


Figure 38. SFDR for Third Harmonic vs. f_{OUT} over Digital Full Scale

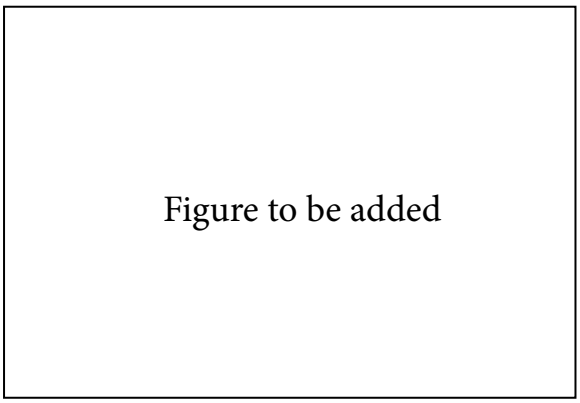


Figure 41. IMD vs. f_{OUT} over DAC I_{OUTFS}

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

Figure to be added

Figure 42. SFDR vs. f_{OUT} over Temperature

Figure to be added

Figure 43. IMD vs. f_{OUT} over Temperature

Figure to be added

Figure 44. Single Tone NSD vs. f_{OUT} over Temperature

Figure to be added

Figure 45. WCDMA NSD vs. f_{OUT} over Temperature

Figure to be added

Figure 46. Single carrier WCDMA at 1887.5 MHz

Figure to be added

Figure 47. Four carrier WCDMA at 1980 MHz

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

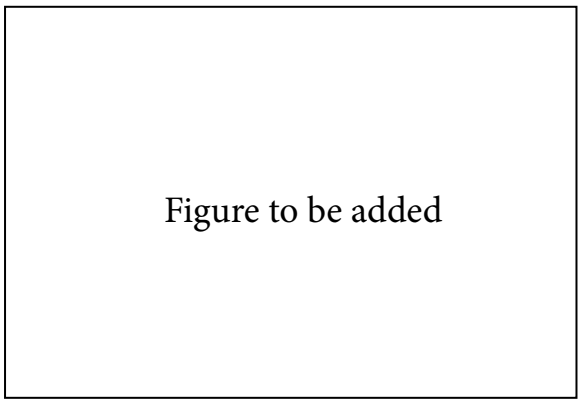


Figure 48. Single Carrier WCDMA ACLR vs. f_{OUT}

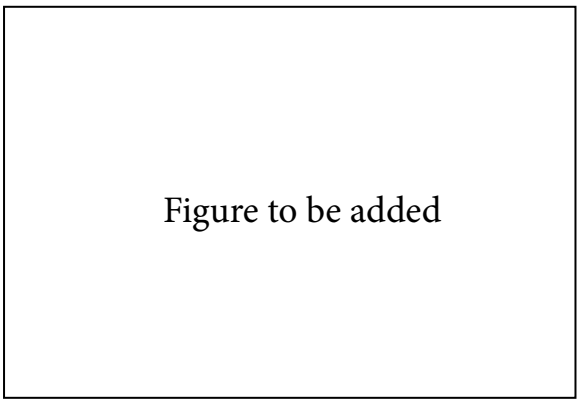


Figure 49. Four Carrier WCDMA ACLR vs. f_{OUT}

DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 33 mA, f_{DAC} = 2.872 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

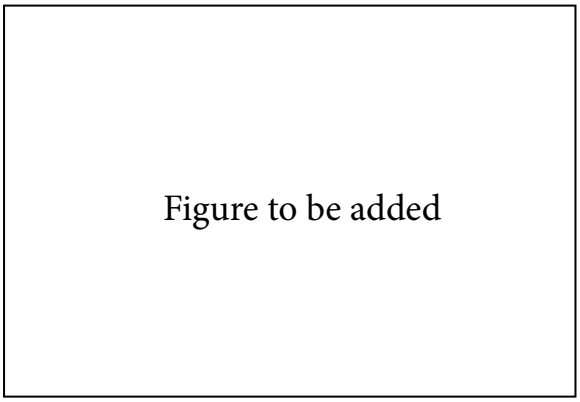


Figure 50. Single carrier at 70 MHz output

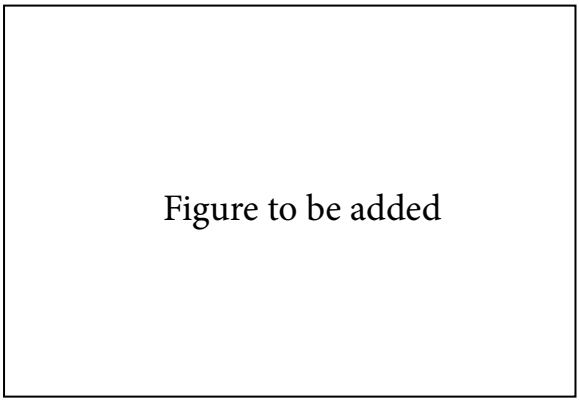


Figure 53. Single carrier at 950 MHz output

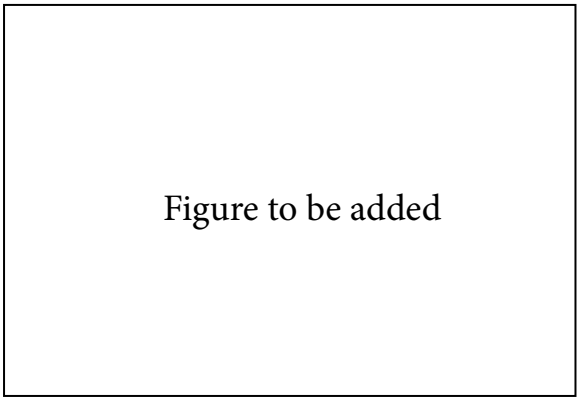


Figure 51. Four carrier at 70 MHz output

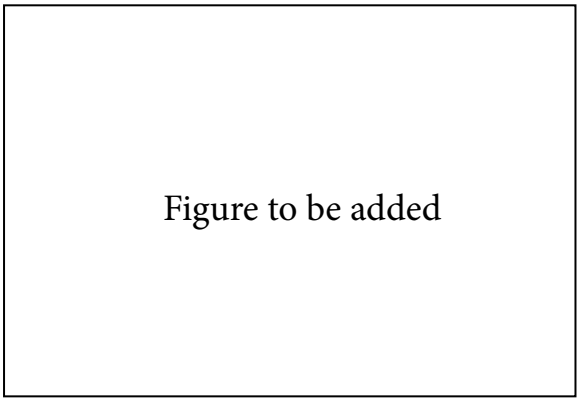


Figure 54. Four carrier at 950 MHz output

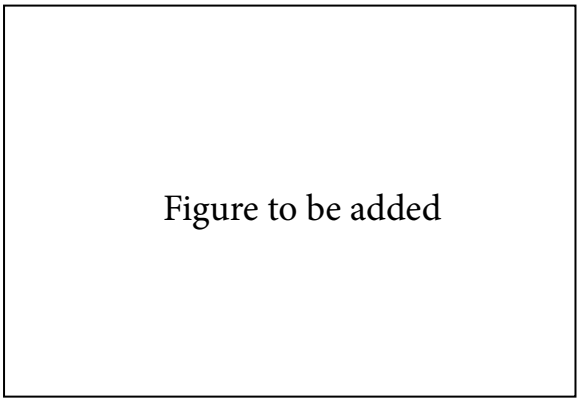


Figure 52. Eight carrier at 70 MHz output

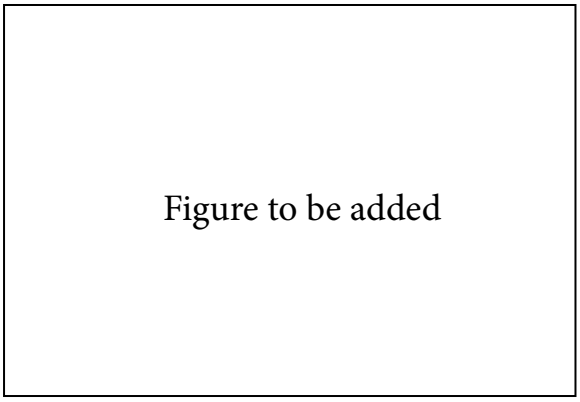


Figure 55. Eight carrier at 950 MHz output

I_{OUTFS} = 33 mA, f_{DAC} = 2.872 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

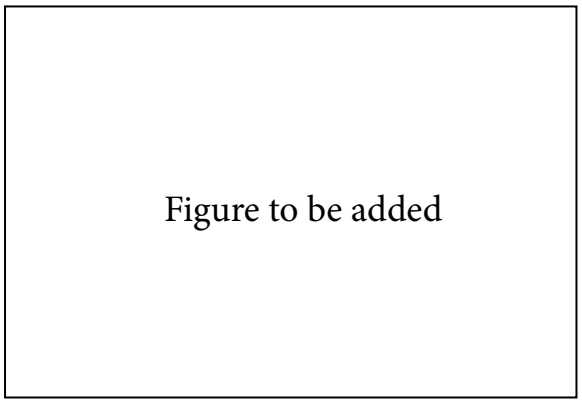


Figure 56. 2nd Harmonic vs. f_{OUT} over number of carriers

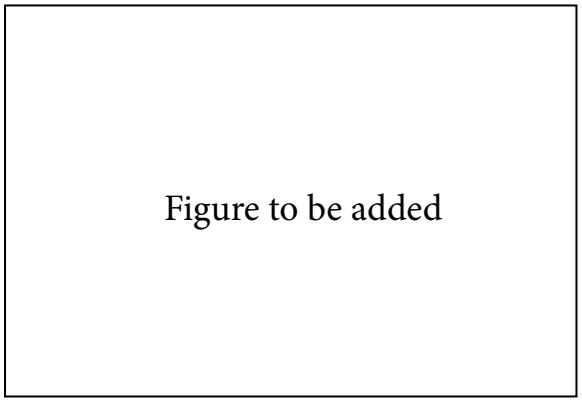


Figure 57. 2nd Harmonic vs. f_{OUT} over number of carriers

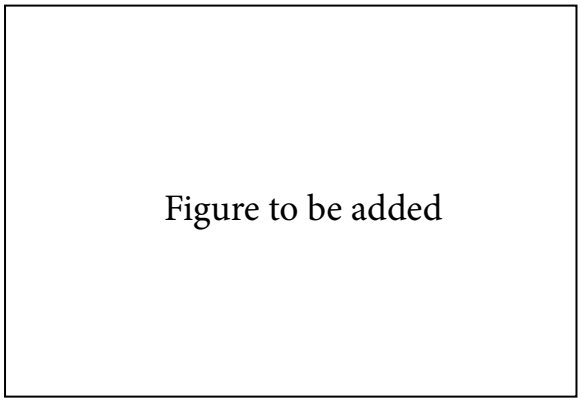


Figure 58. Single carrier ACLR vs. f_{OUT}

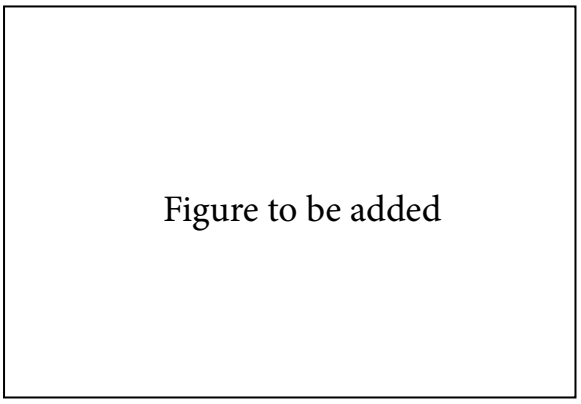


Figure 59. Four carrier ACLR vs. f_{OUT}

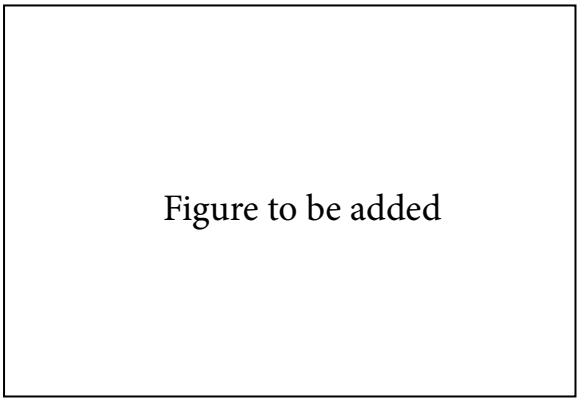


Figure 60. Eight carrier ACLR vs. f_{OUT}

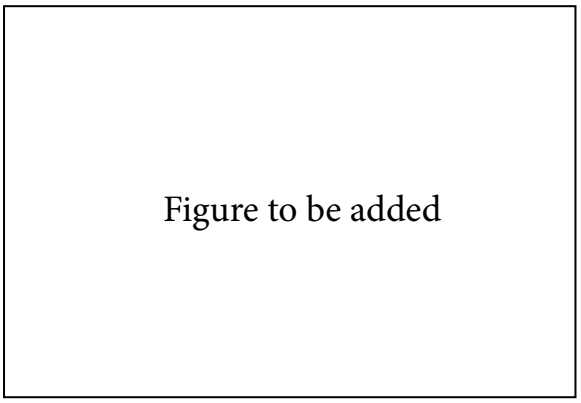


Figure 61. 16- carrier ACLR vs. f_{OUT}

I_{OUTFS} = 33 mA, f_{DAC} = 2.872 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

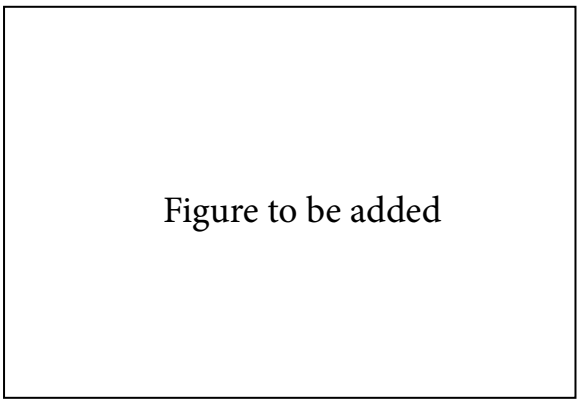


Figure 62. 32-, 64- 128- carrier ACLR vs. f_{OUT}

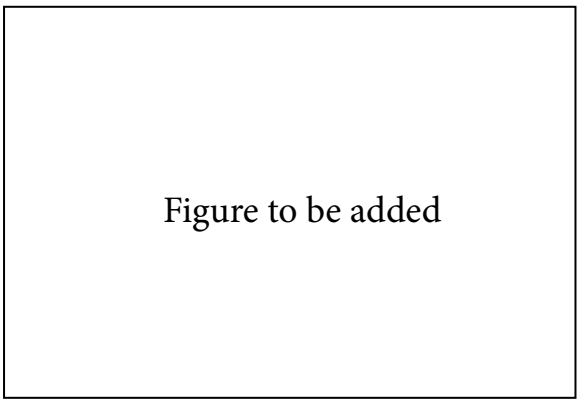


Figure 63. Gap channel ACLR at 900 MHz

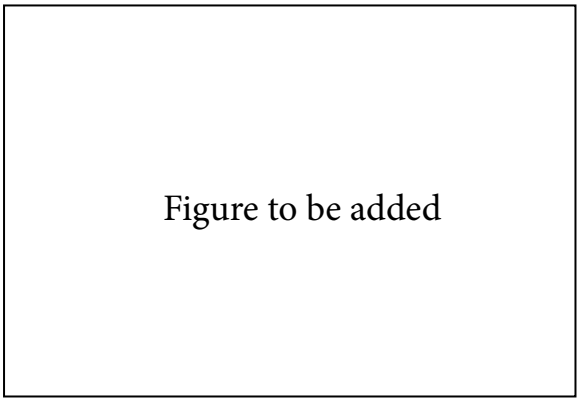


Figure 64. Gap channel ACLR vs. f_{OUT}

TYPICAL PERFORMANCE CHARACTERISTICS – AD9129

STATIC LINEARITY

I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

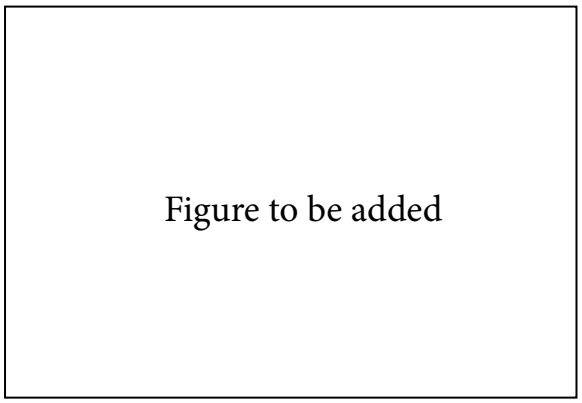


Figure 65. Typical INL, 11 mA at 25°C

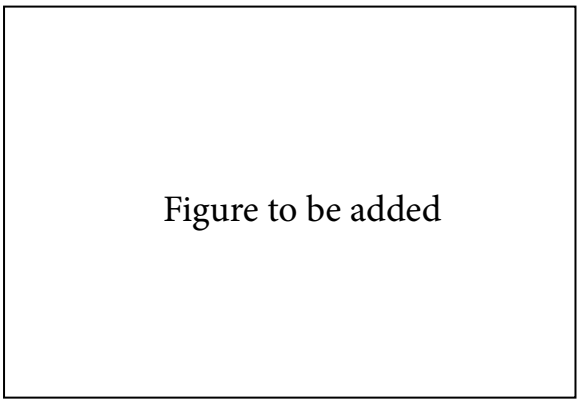


Figure 68. Typical DNL, 11 mA at 25°C

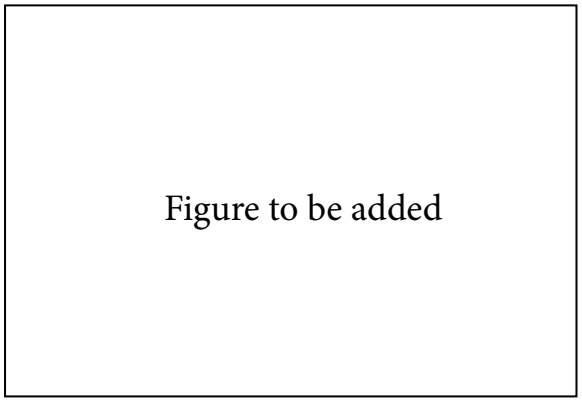


Figure 66. Typical INL, 22 mA at 25°C

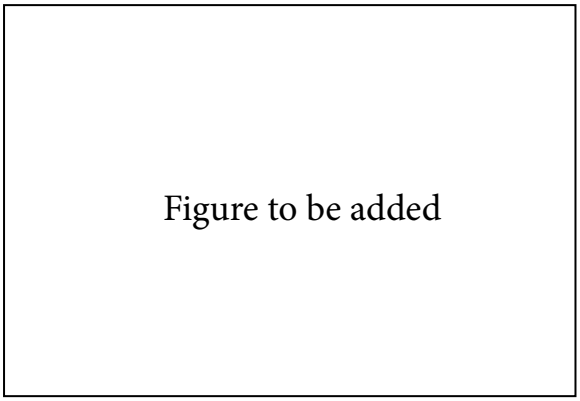


Figure 69. Typical DNL, 22 mA at 25°C

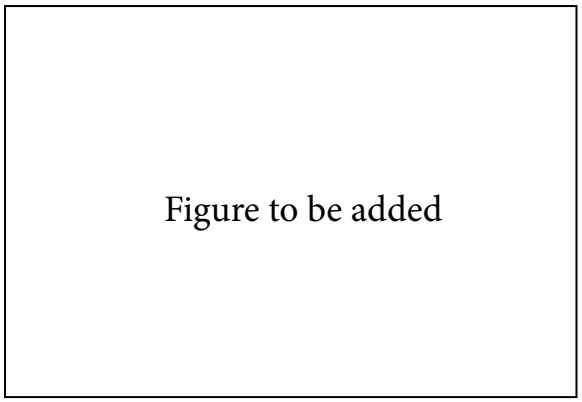


Figure 67. Typical INL, 33 mA at 25°C

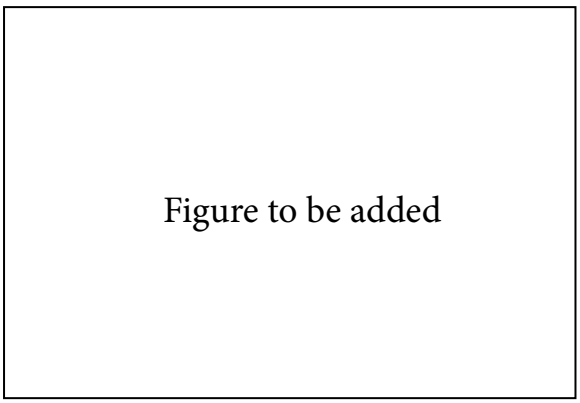


Figure 70. Typical DNL, 33 mA at 25°C

AC (NORMAL MODE)

I_{OUTFS} = 28 mA, nominal supplies, f_{DAC} = 2.6 GSPS, T_A = 25°C, unless otherwise noted.

Figure to be added

Figure 71. Single Tone Spectrum at f_{OUT} = 70 MHz

Figure to be added

Figure 72. Single-Tone Spectrum at f_{OUT} = 1000 MHz

Figure to be added

Figure 73. SFDR vs. f_{OUT} over f_{DAC}

Figure to be added

Figure 74. IMD vs. f_{OUT} over f_{DAC}

Figure to be added

Figure 75. Single-Tone NSD over f_{OUT}

Figure to be added

Figure 76. WCDMA NSD over f_{OUT}

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

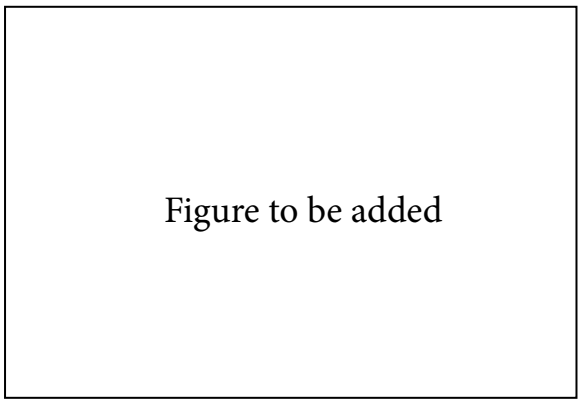


Figure 77. SFDR vs. f_{OUT} over Digital Full Scale

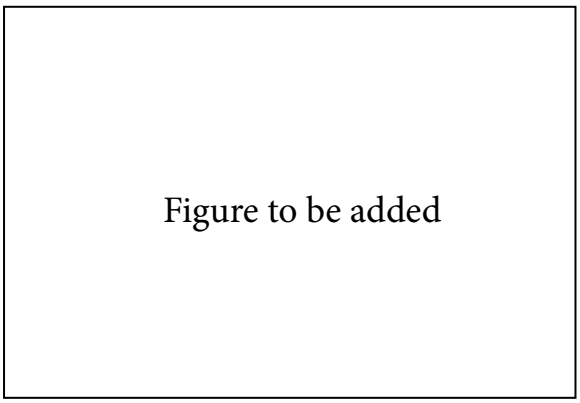


Figure 80. IMD vs. f_{OUT} over Digital Full Scale

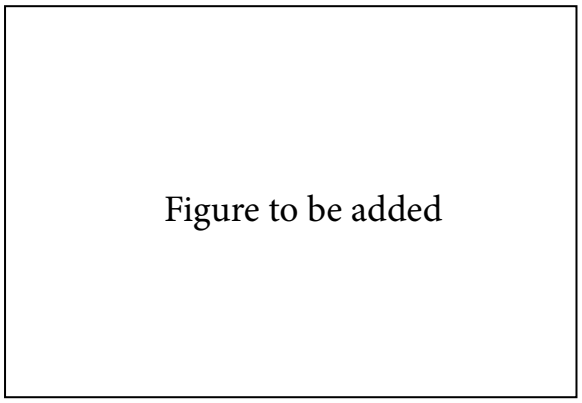


Figure 78. SFDR for Second Harmonic vs. f_{OUT} over Digital Full Scale

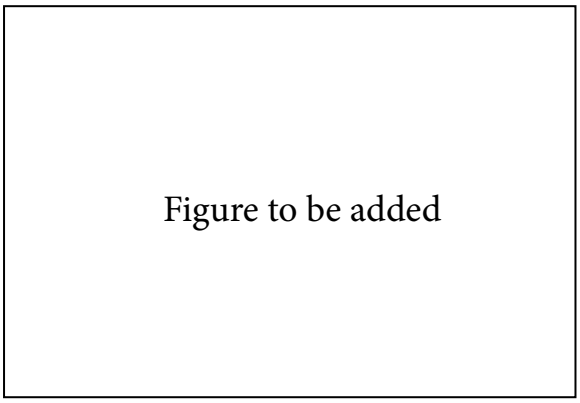


Figure 81. SFDR vs. f_{OUT} over DAC I_{OUTFS}

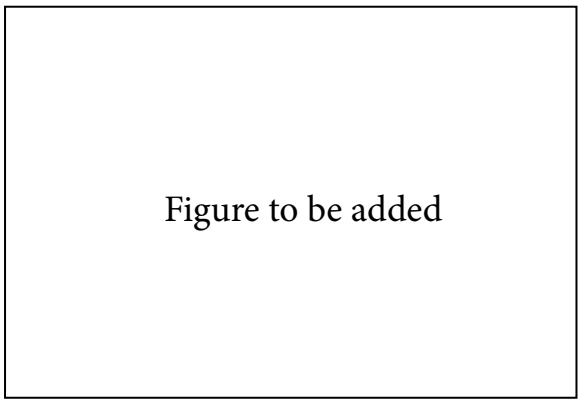


Figure 79. SFDR for Third Harmonic vs. f_{OUT} over Digital Full Scale

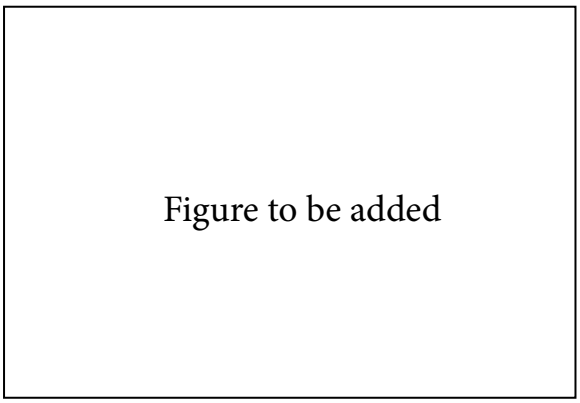


Figure 82. IMD vs. f_{OUT} over DAC I_{OUTFS}

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

Figure to be added

Figure 83. SFDR vs. f_{OUT} over Temperature

Figure to be added

Figure 84. IMD vs. f_{OUT} over Temperature

Figure to be added

Figure 85. Single Tone NSD vs. f_{OUT} over Temperature

Figure to be added

Figure 86. WCDMA NSD vs. f_{OUT} over Temperature

Figure to be added

Figure 87. Single carrier WCDMA at 877.5 MHz

Figure to be added

Figure 88. Two carrier WCDMA at 875 MHz

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

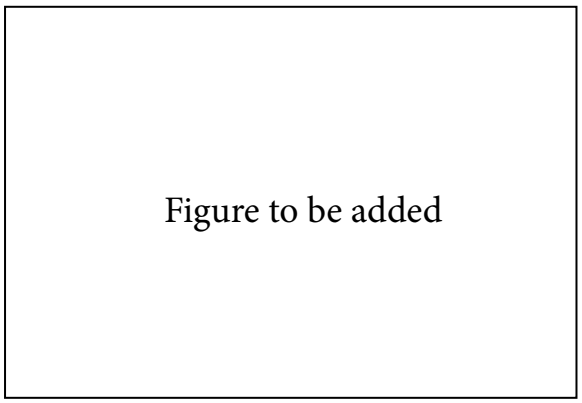


Figure 89. Single Carrier WCDMA ACLR vs. f_{OUT}

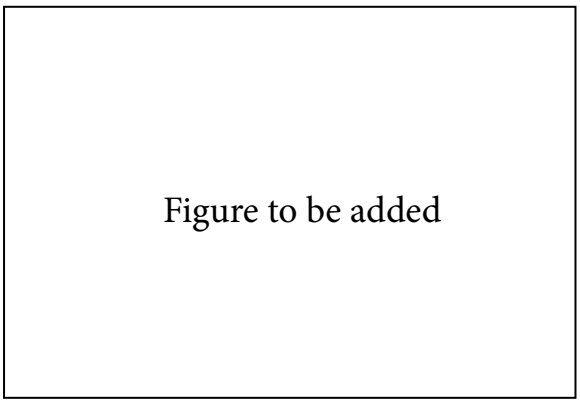


Figure 90. Two Carrier WCDMA ACLR vs. f_{OUT}

AC (MIX-MODE)

I_{OUTFS} = 28 mA, nominal supplies, f_{DAC} = 2.6 GSPS, T_A = 25°C, unless otherwise noted.

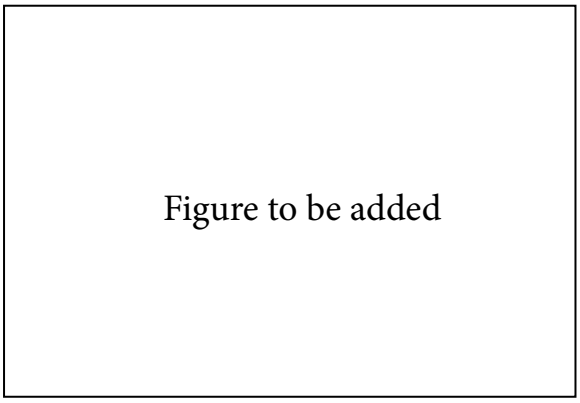


Figure 91. Single Tone Spectrum at f_{OUT} = 2350 MHz

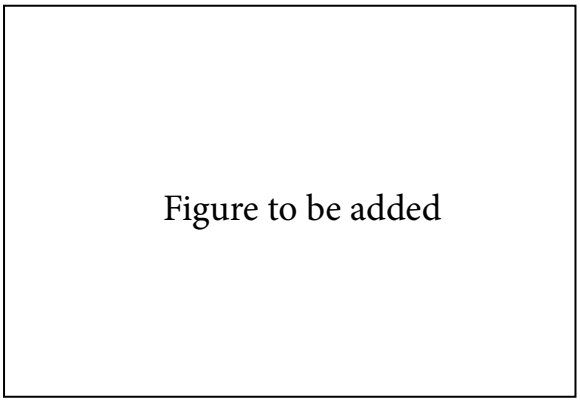


Figure 94. IMD vs. f_{OUT} over f_{DAC}

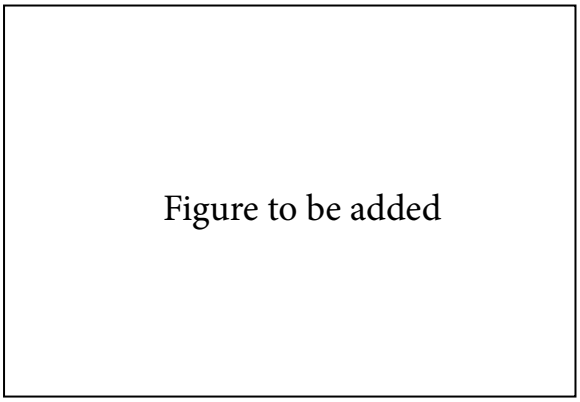


Figure 92. Single-Tone Spectrum at f_{OUT} = 1600 MHz

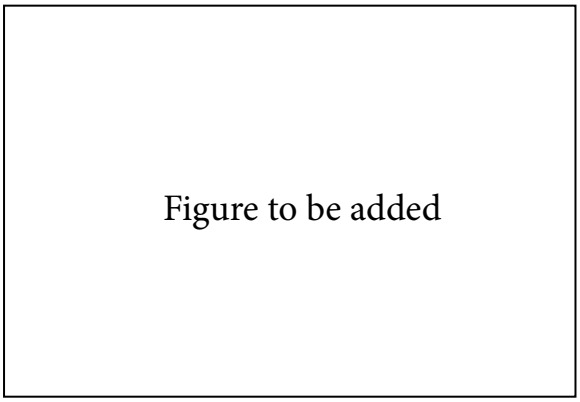


Figure 95. Single-Tone NSD over f_{OUT}

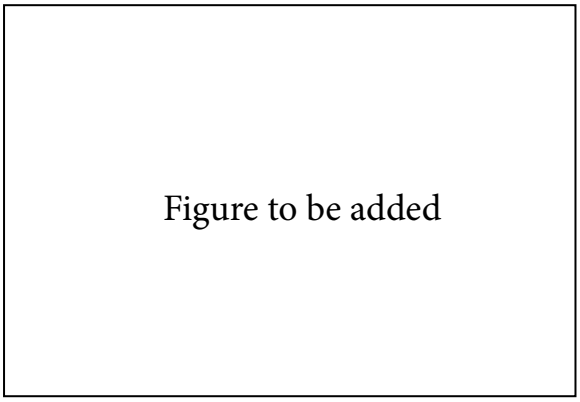


Figure 93. SFDR vs. f_{OUT} over f_{DAC}

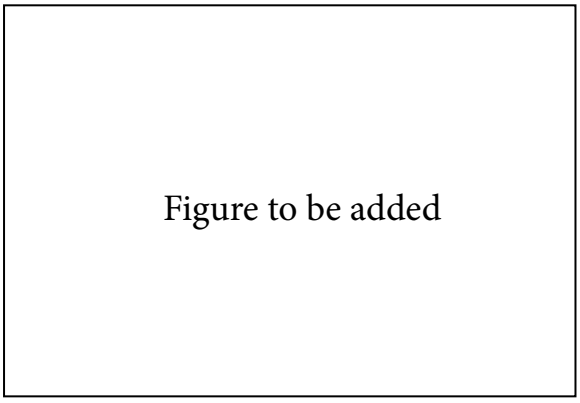


Figure 96. WCDMA NSD over f_{OUT}

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

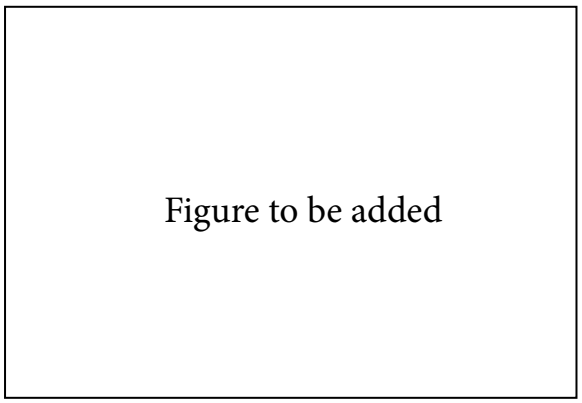


Figure 97. SFDR vs. f_{OUT} over Digital Full Scale

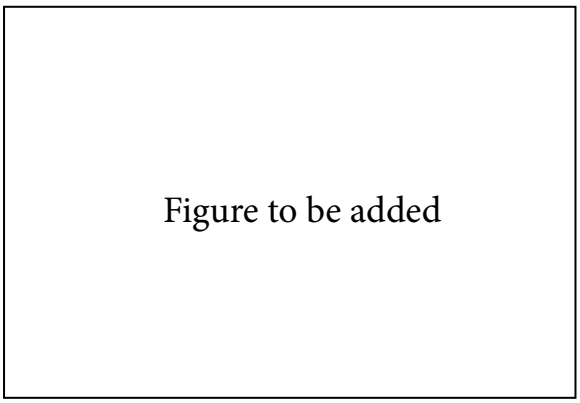


Figure 100. IMD vs. f_{OUT} over Digital Full Scale

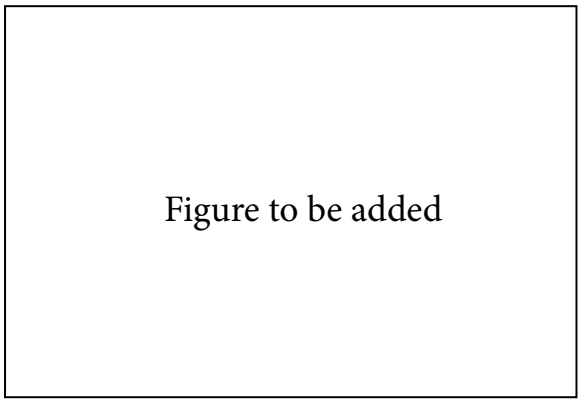


Figure 98. SFDR for Second Harmonic vs. f_{OUT} over Digital Full Scale

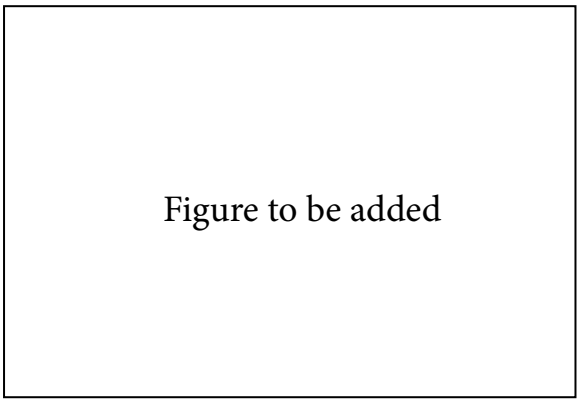


Figure 101. SFDR vs. f_{OUT} over DAC I_{OUTFS}

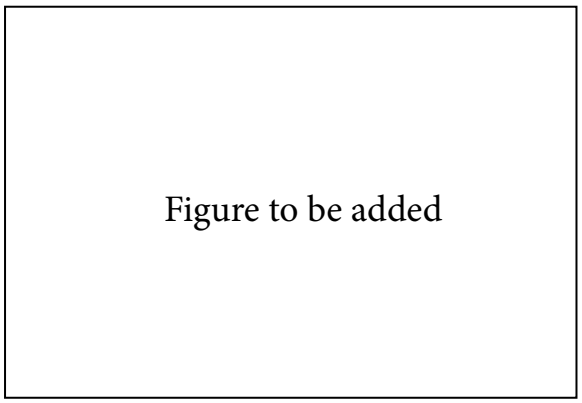


Figure 99. SFDR for Third Harmonic vs. f_{OUT} over Digital Full Scale

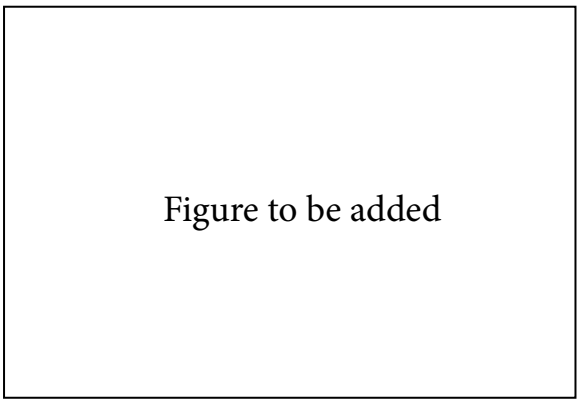


Figure 102. IMD vs. f_{OUT} over DAC I_{OUTFS}

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

Figure to be added

Figure 103. SFDR vs. f_{OUT} over Temperature

Figure to be added

Figure 104. IMD vs. f_{OUT} over Temperature

Figure to be added

Figure 105. Single Tone NSD vs. f_{OUT} over Temperature

Figure to be added

Figure 106. WCDMA NSD vs. f_{OUT} over Temperature

Figure to be added

Figure 107. Single carrier WCDMA at 1887.5 MHz

Figure to be added

Figure 108. Four carrier WCDMA at 1980 MHz

f_{DAC} = 2.6 GSPS, I_{OUTFS} = 28 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

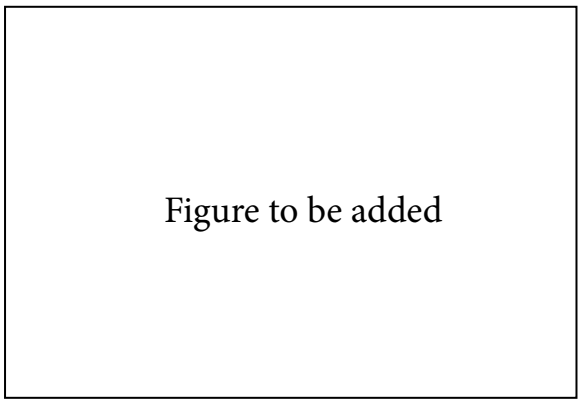


Figure 109. Single Carrier WCDMA ACLR vs. f_{OUT}

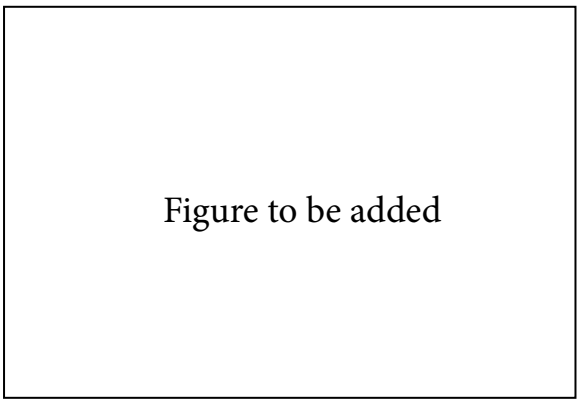


Figure 110. Four Carrier WCDMA ACLR vs. f_{OUT}

DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 33 mA, f_{DAC} = 2.872 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

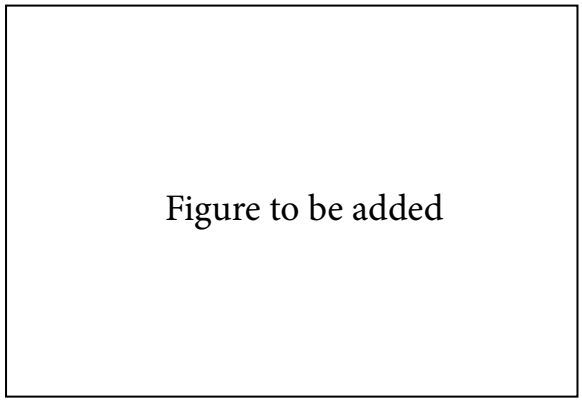


Figure 111. Single carrier at 70 MHz output

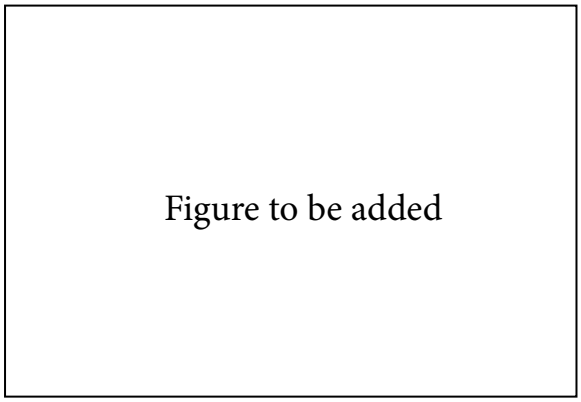


Figure 114. Single carrier at 950 MHz output

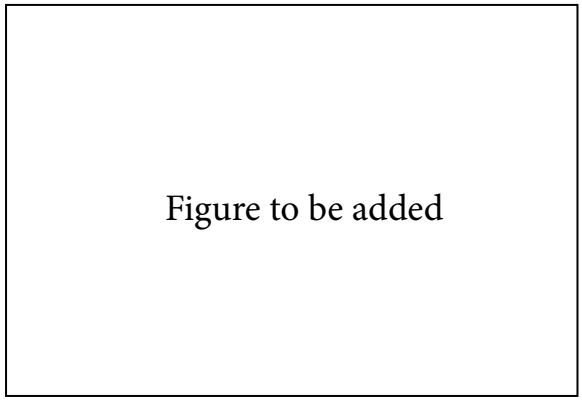


Figure 112. Four carrier at 70 MHz output

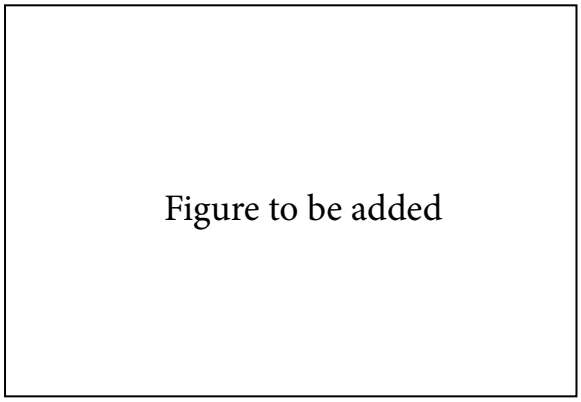


Figure 115. Four carrier at 950 MHz output

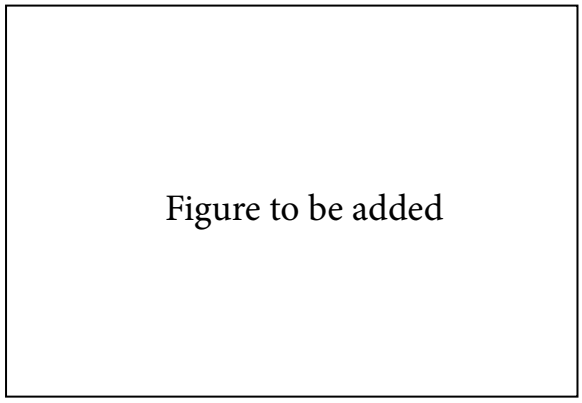


Figure 113. Eight carrier at 70 MHz output

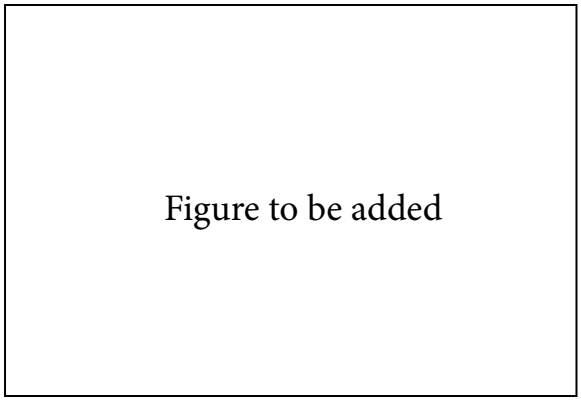


Figure 116. Eight carrier at 950 MHz output

I_{OUTFS} = 33 mA, f_{DAC} = 2.872 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

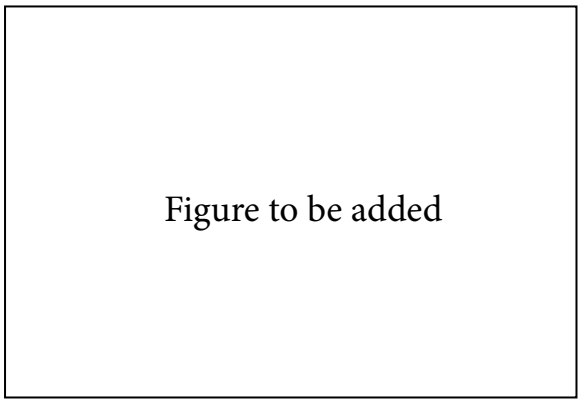


Figure 117. 2nd Harmonic vs. f_{OUT} over number of carriers

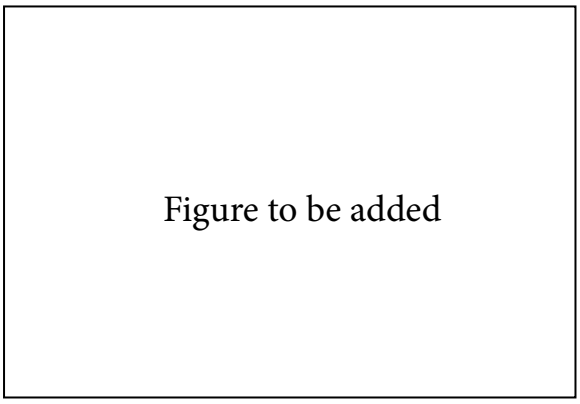


Figure 120. Four carrier ACLR vs. f_{OUT}

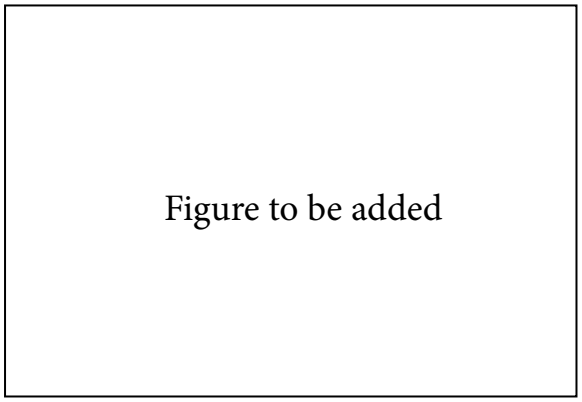


Figure 118. 2nd Harmonic vs. f_{OUT} over number of carriers

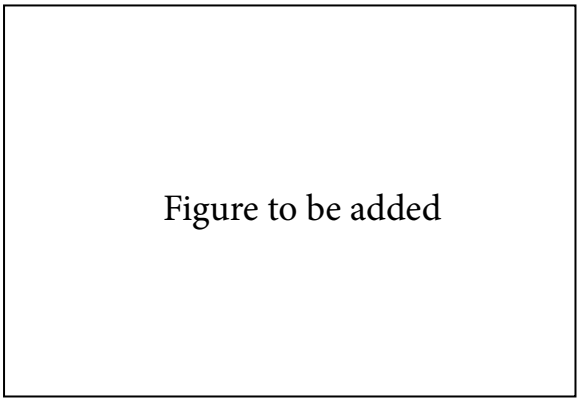


Figure 121. Eight carrier ACLR vs. f_{OUT}

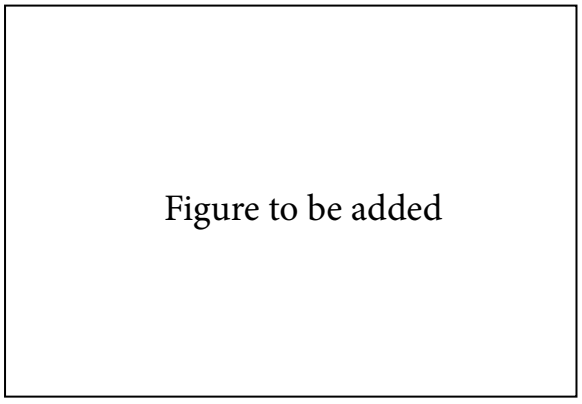


Figure 119. Single carrier ACLR vs. f_{OUT}

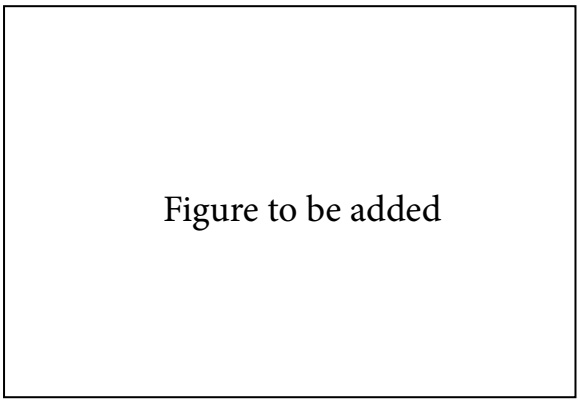


Figure 122. 16- carrier ACLR vs. f_{OUT}

I_{OUTFS} = 33 mA, f_{DAC} = 2.872 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

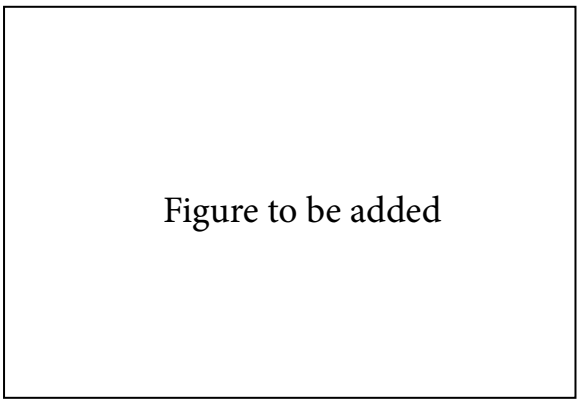


Figure 123. 32-, 64- 128- carrier ACLR vs. f_{OUT}

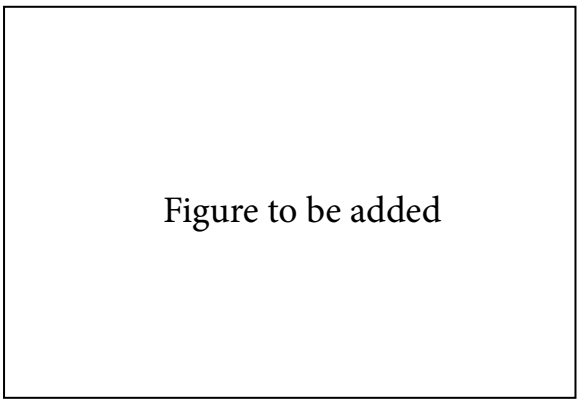


Figure 124. Gap channel ACLR at 900 MHz

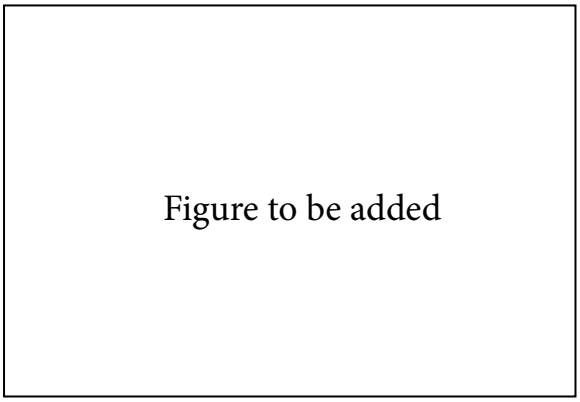


Figure 125. Gap channel ACLR vs. f_{OUT}

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
The maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
The measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called the offset error. For IOUTP, 0 mA output is expected when the inputs are all 0s. For IOUTN, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1 minus the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Spurious-Free Dynamic Range
The difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Noise Spectral Density (NSD)
NSD is the converter noise power per unit of bandwidth. This is usually specified in dBm/Hz in the presence of a 0 dBm full-scale signal.

Adjacent Channel Leakage Ratio (ACLR)
The adjacent channel leakage (power) ratio is a ratio, in dBc, between the measured power within a channel relative to its adjacent channels.

Modulation Error Ratio (MER)
Modulated signals create a discrete set of output values referred to as a constellation. Each symbol creates an output signal corresponding to one point on the constellation. MER is a measure of the discrepancy between the average output symbol magnitude and the rms error magnitude of the individual symbol.

Intermodulation Distortion (IMD)
IMD is the result of two or more signals at different frequencies mixing together. Many products are created according to the formula aF1± bF2, where a and b are integer values.

THEORY OF OPERATION

The AD9119/AD9129 is a 11-bit/14-bit DAC that operates at an update rate of up to 2.8 GSPS. Due to internal timing requirements, the minimum allowable sample rate is 1400 MSPS. Input data is sampled through two 11-bit/14-bit LVDS ports that are internally multiplexed. Each port has its own data inputs, but both ports share a common DCI input. The LVDS inputs meet the IEEE-1596 specification with the exception of input hysteresis, which is not guaranteed over all process corners. Each DCI input runs at one-quarter the input data rate in a double data rate (DDR) format. Each edge of DCI is used to transfer data into the AD9119/AD9129.

The DACCLK_N/DACCLK_P inputs directly drive the DAC core to minimize clock jitter. The DACCLK signal is divided by 4 then output as the DCO for each port. The DCO signal can be used to clock the data source. The DAC expects DDR LVDS data (DB0[13:0], DB1[13:0]), with each channel aligned with the single DDR data input clock (DCI).

Control of the AD9119/AD9129 functions is via a serial peripheral interface (SPI).

SERIAL PERIPHERAL INTERFACE

The AD9119/AD9129 serial port is a flexible, synchronous serial communications port, allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including the Motorola® SPI and the Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9119/AD9129. Most significant bit first (MSB-first) or least significant bit first (LSB-first) transfer formats are supported. The AD9119/AD9129 serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for input/output (SDIO/SDO).

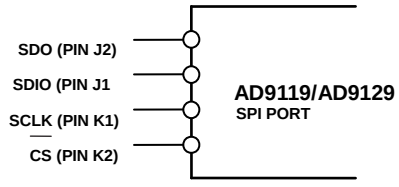


Figure 126. AD9119/AD9129 SPI Port

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communication cycle with the AD9119/AD9129. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9119/AD9129 coincident with the first eight SCLK rising edges. The instruction byte provides the AD9119/AD9129 serial port controller with information about the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9119/AD9129.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9119/AD9129 and the system controller. Phase 2 of the communication cycle is a transfer of one byte only. Single-byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte. $\overline{CS}$ (chip select) can be raised after each sequence of eight bits (except the last byte) to stall the bus. The serial transfer resumes when $\overline{CS}$ is lowered. Stalling on nonbyte boundaries resets the SPI.

INSTRUCTION MODE (8-BIT INSTRUCTION)

The instruction byte is shown in the following table.

MSB **LSB**

I7	I6	I5	I4	I3	I2	I1	I0
R/W	A6	A5	A4	A3	A2	A1	A0

R/W, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation, the data transfer cycle. A6 to A0 (Bit 6 through Bit 0 of the instruction byte) determine which register is accessed during the data transfer portion of the communications cycle.

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9119/AD9129 and to run the internal state machines. The maximum frequency of SCLK is 20 MHz. All data input to the AD9119/AD9129 is registered on the rising edge of SCLK. All data is driven out of the AD9119/AD9129 on the rising edge of SCLK.

$\overline{CS}$—Chip Select

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O

Data is always written into the AD9119/AD9129 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by SDIO_DIR at Register 0x00, Bit 7. The default is Logic 0, which configures the SDIO pin as unidirectional.

SDO—Serial Data Out

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9119/AD9129 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB TRANSFERS

The AD9119/AD9129 serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by LSB/MSB at Register 0x00, Bit 6. The default is MSB first (LSB/MSB = 0). When LSB/MSB = 0 (MSB first), the instruction and data bytes must be written from the most significant bit to the least significant bit.

When LSB/MSB = 1 (LSB first), the instruction and data bytes must be written from the least significant bit to the most significant bit.

SERIAL PORT CONFIGURATION

The AD9119/AD9129 serial port configuration is controlled by Register 0x00, Bits[7:5]. Note that the configuration changes immediately upon writing to the last bit of the register. When setting the software reset (Register 0x00, Bit 5), all registers are set to their default values except Register 0x00, which remains unchanged.

In the event of unexpected programming sequences, the AD9119/AD9129 SPI can become inaccessible. For example, if user code inadvertently changes the LSB/MSB bit, the following bits experience unexpected results. The SPI can be returned to a known state by writing an incomplete byte (1 to 7 bits) of all 0s followed by three bytes of 0x00. This returns to the MSB-first instructions (Register 0 x00 = 0x00) so that the device can be reinitialized.

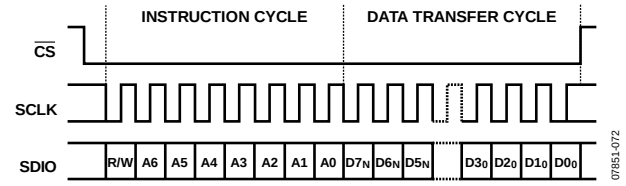


Figure 127. Serial Register Interface Timing, MSB-First Write

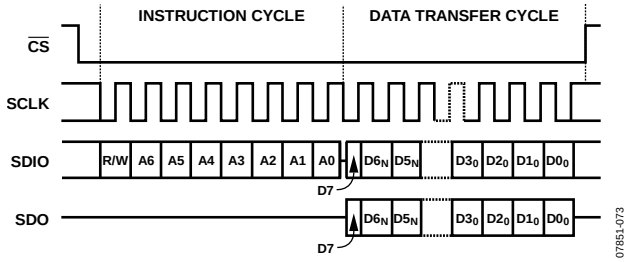


Figure 128. Serial Register Interface Timing, MSB-First Read

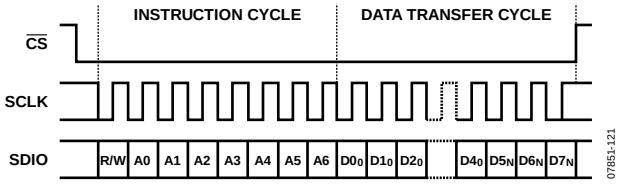


Figure 129. Serial Register Interface Timing, LSB-First Write

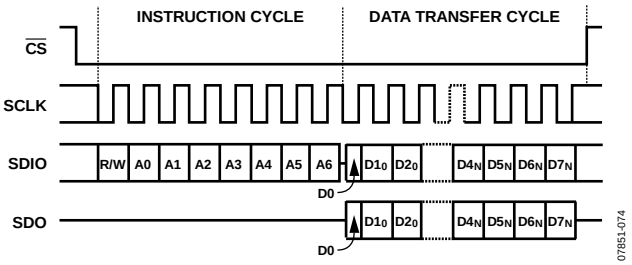


Figure 130. Serial Register Interface Timing, LSB-First Read

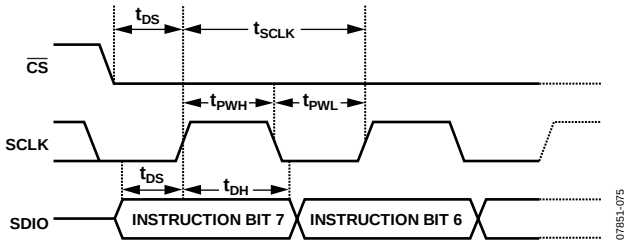


Figure 131. Timing Diagram for an SPI Register Write

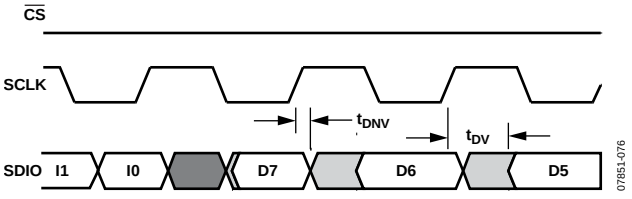


Figure 132. Timing Diagram for an SPI Register Read

After the last instruction bit is written to the SDIO pin, the driving signal must be set to a high impedance in time for the bus to turn around. The serial output data from the AD9119/AD9129 is enabled by the falling edge of SCLK. This causes the first output data bit to be shorter than the remaining data bits, as shown in Figure 79. To assure proper reading of data, read the SDIO or SDO pin prior to changing the SCLK from low to high. Due to the more complex multibyte protocol, multiple AD9119/AD9129 devices cannot be daisy-chained on the SPI bus. Multiple DACs should be controlled by independent $\overline{CS}$ signals.

THEORY OF OPERATION

The AD9119/AD9129 is a 11-bit/14-bit TxDAC capable of reconstructing signal bandwidths up to 1.4 GHz while operating with an input data rate up to 2.8 GSPS. Figure 133 shows a top-level functional diagram of the AD9119/AD9129. A high performance NMOS DAC delivers a signal dependent, differential current to a balanced external load referenced a nominal 1.8 V analog supply. The DAC's current source array is referenced to an external -1.5 V supply and its full-scale current, IOUTFS, can be adjusted over a 9.5 to 34.4 mA span.

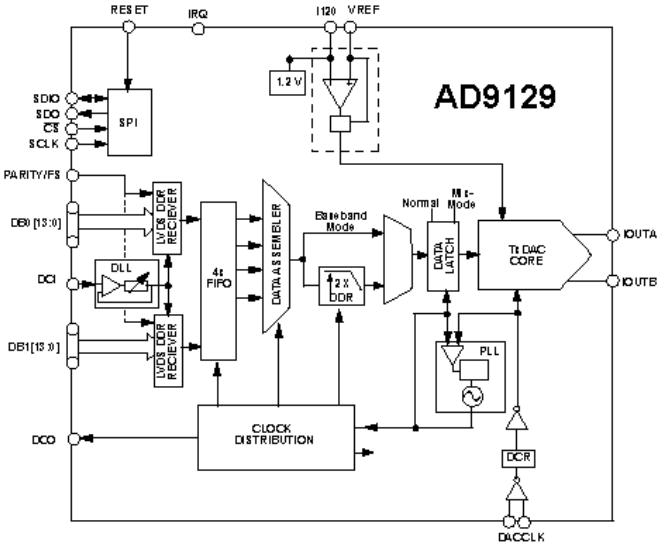


Figure 133.Functional Block diagram of the AD9119/AD9129

A low jitter differential clock receiver is used to square up the signal appearing at the DACCLK input that sets the TxDAC's update rate. The differential clock receiver can accept sinusoidal signals with negligible jitter penalty if the slew rate is maintained greater than ??TBD V/ns. A duty cycle restorer (DCR) following the clock receiver ensures near 50% duty-cycle to the subsequent circuitry. The output of the DCR serves as the master clock and is routed directly to the TxDAC as well as a clock distribution block that generates all critical internal and external clocks. The clock source quality defined by its phase noise characteristics, jitter, and drive capability are important considerations in maintaining optimum AC performance.

The AD9119/AD9129 supports a source synchronous, LVDS double data-rate (DDR) data interface to the host processor. Two 11-bit/14-bit LVDS data ports (DB0 and DB1) are used to sample de-interleaved data from the host on the *rising* and *falling* edge of the host's DCI clock. This effectively reduces the bus interface speed to ½ the data rate (i.e. $F_{DATA}/2$) with the DCI clock operating at $F_{DATA}/4$. An optional parity bit can also be sent along with the data to enhance the robustness of the interface. In this case, a counter is available to count parity errors and generate an interrupt request (IRQ) once a programmable threshold has been exceeded.

The AD9119/AD9129 provides the host with a DCO clock that is equal to the DCI clock frequency to establish synchronous operation. A delay-lock-loop (DLL) with programmable phase offset is used to generate an internal sampling clock with optimum edge placement for the input data latches of the LVDS DDR Receivers. Once data is latched into the AD9119/AD9129, an 8-sample deep FIFO is used to hand-off the data between the host and AD9119/AD9129's clock domains. The FIFO can be reset with an external synchronization signal, FS, to ensure consistent pipeline latency. The pipeline delay from a sample being latched into the data port to when it appears at the DAC output varies depending on the chosen configuration. (See Pipeline Delay (Latency))

The de-interleaved data is reassembled into its original data stream after passing into the AD9119/AD9129's internal clock domain. Since the TxDAC's quad switch architecture updates its output on both the *rising* and *falling* edge (i.e. dual edge clocking) of the DACCLK, the following additional modes of operation are available. A 2x interpolation filter can be selected to increase the effective DAC update rate (FDAC) to be 2x the input data rate hence simplifying the analog post filtering requirements and reducing effects of alias harmonics in the desired baseband region. Also available is a mix-mode option which essentially generates the complement sample on the *falling* edge such that the original Nyquist spectrum is shifted to f_{DACCLK} with the DAC's Sinc null falling at 2* f_{DACCLK}.

The digital handoff between the digital domain and mixed-signal domain of a high speed DAC is critical in preserving its output dynamic range. A phase locked loop (PLL) with programmable phase offset is used to optimize the timing handoff between these two clock domains. State machines are used to initialize both the DLL and the PLL during the initial boot sequence after receiving a stable DACCLK signal. Once the two loops are initialized, they will maintain optimum timing alignment over temperature, time and power supply variation. The AD9119/AD9129 also provides IRQ capability to monitor the DLL, the PLL, and other internal circuitry.

LVDS DATA PORT INTERFACE

The AD9119/AD9129 can operate with input data rates up to 2.8 GSPS. A source synchronous LVDS interface is used between the host and AD9119/AD9129 to achieve these high data rates while simplifying the interface. Referring to Figure 134, the host feeds the AD9119/AD9129 with de-interleaved input data into two 11-bit/14-bit LVDS data ports (DB01 and DB1) at ½ the DAC clock rate (i.e. $f_{DACCLK}/2$). Along with the input data, the host provides an embedded DDR (Double Data Rate) data clock input, (DCI) at $f_{DACCLK}/4$.

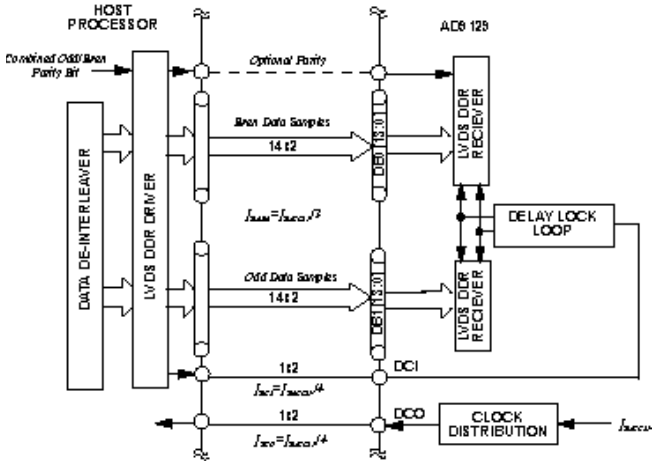


Figure 134. Recommended Digital Interface between AD9119/AD9129 and Host Processor.

A delay lock loop (DLL) circuit designed to operate with DCI clock rates between 250-700 MHz is used to generate a phase shifted version of DCI, called DSC (Data Sampling Clock), to register the input data on both the rising and falling edges. Referring toFigure 135, the DCI clock edges must be coincident with the data bit transitions with minimum skew, jitter and inter-symbol interference. The nominal sampling point of the input data occurs in the middle of the DCI clock edges since this corresponds to the center of the data eye. This is also equivalent to a nominal phase shift of 90° of the DCI clock.

The data timing requirements are defined by a Data Valid Window (DVW) that is dependent on the data clock input skew, input data jitter, and the variations of the DLL delay line across delay settings. The DVW is defined as

$$DVW = t_{Data\ Period} - t_{DCI\ skew} - t_{Data\ Jitter}$$

The available margin for data interface timing is therefore given by

$$T_{Margin} = DVW - t_{DSC\ Setup\ and\ Hold}$$

The timing margin allows tuning of the Delay-Locked Loop (DLL) delay setting either automatically or in Manual mode. This is illustrated inFigure 135.

From the figure, it can be seen that the ideal location for the DSC signal is 90 degrees out of phase from the DCI input. However, due to skew of the DCI relative to the data, it may be necessary to change the DSC phase offset in order to sample the data at the center of its eye diagram.

Table 10 shows the needed times to calculate the DVW and therefore the amount of margin available for tuning of the DSC sampling point can be determined.

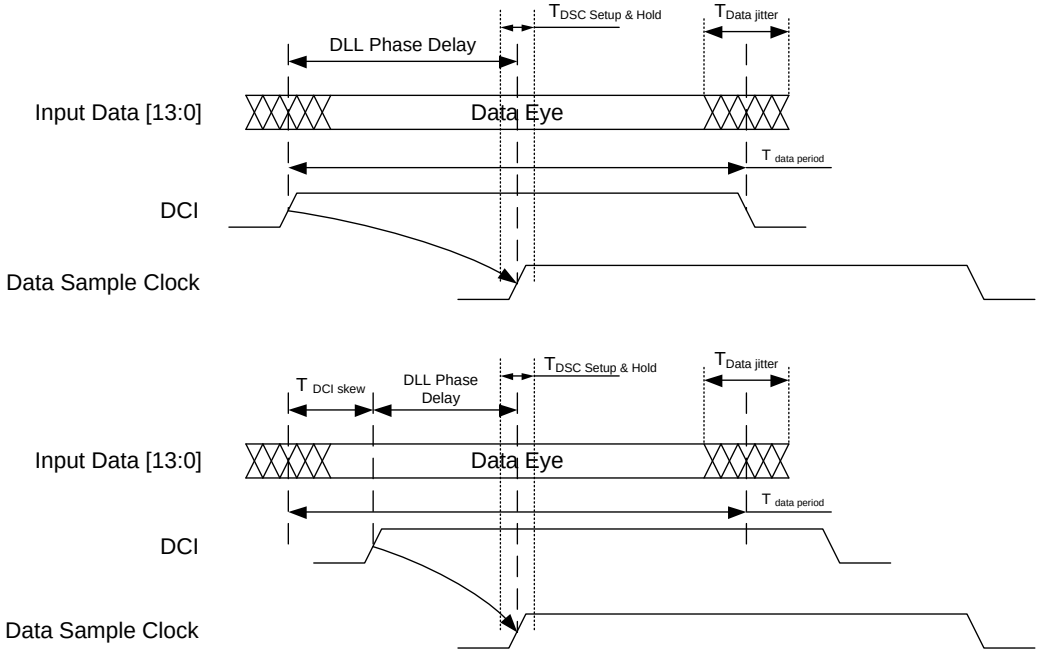


Figure 135. LVDS data port timing requirements

Table 10. Data Port Set and Hold Time Window (MAX)

		Data Port Set and Hold Time Window, $t_{DSC\ Setup\ \&\ Hold}$, (ps), at DLL Phase															
F_{DAC}	**Time**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
1000 MHz	t_S																
	t_H																
1600 MHz	t_S																
	t_H																
2300 MHz	t_S																
	t_H																
2800 MHz	t_S																
	t_H																

NOTE 1: **BOLD** NUMBERS INDICATE GUARANTEED NUMBERS.

NOTE 2: THE TABLE SHOWS CHARACTERIZATION DATA FOR SELECTED F_{DAC} FREQUENCIES. OTHER FREQUENCIES ARE POSSIBLE AND THE TABLE CAN BE USED TO ESTIMATE PERFORMANCE

Maximizing the opening of the eye in both the DCI and data signals improves the reliability of the data port interface. Differential controlled impedance traces of equal length (i.e. delay) should be used between the host processor and AD9119/AD9129 input. To ensure coincident transitions with the data bits, the DCI signal should be implemented as an additional data line with an alternating (010101…) bit sequence from the same output drivers used for the data.

For synchronous operation between the host and AD9119/AD9129, the AD9119/AD9129 provides a data clock output, DCO, to the host at the same rate as DCI (i.e. $f_{DACCLK}/4$). Note, the DCI signal can have arbitrary phase alignment with respect to the DCO since the AD9119/AD9129's DLL ensures proper data hand-off between the two clock domains (i.e. host processors and AD9119/AD9129's internal digital core).

The default reset state of the AD9119/AD9129 is to have the DCO signal disabled. To enable it, write a '1' to register 0x0C[6].The DCO output level is controlled in register 0x7C[7:6]. The default setting is '01', or 2.8 mA, but it can be increased to as high as 4 mA ('11') if higher swing is necessary.

The DCI signal is AC-coupled internally, and so a possibility exists that removing the DCI signal could cause DAC output "chatter" due to randomness on the DCI input. To avoid this, it is recommended that the DAC output is disabled whenever the DCI signal is not present. To do this, program the DAC output current power down bit in register 0x01[6] to '1'. When DCI is again present, the DAC output can be enabled by programming the register 0x01[6] bit to '0'. The DAC output will power up in about 2 usec.

The status of the DLL can be polled by reading the Data Status register at address 0x0E. Bit 0 indicates the DLL is running and attempting lock, and bit 7 will be '1' when the DLL has locked. Bit 2 is '1' when a valid Data Clock In is detected. The warning bits in [6:3] can be used as indicators that the DAC may be operating in a non-ideal location in the delay line. Note that these bits are read at the SPI port speed, which is much slower than the actual speed of the DLL. This means they can only show a snapshot of what is happening as opposed to giving real-time feedback.

Parity

The data interface can be continuously monitored by enabling the PARITY bit feature in Reg 0x5C[7] and configuring the Frame/Parity bit (B14) as Parity by setting bit 0x07[0] = 1.. In this case, the host would send a PARITY bit along with each data sample. This bit represents the XOR value of data bits from the combined de-interleaved samples (i.e. Even+Odd).

If a parity error occurs, the parity error counter (Register 0x5D or 0x5E) is incremented. Parity errors on the bits sampled by the rising edge of DCI will increment the Rising Edge Parity counter (Reg 0x5D) and set the ParErrRis bit (0x5C[0]). Parity errors on the bits sampled by the falling edge of DCI will increment the Falling Edge Parity counter (Rex 0x5E) and set the ParErrFal bit (Reg 0x5C[1]). The parity counter continues to accumulate until it is cleared or until it reaches a maximum value of 255. The count can be cleared by writing a 1 to Register 0x5C[5].

An IRQ can be enabled to trigger when a parity error occurs by writing a 1 to Register 0x04[2] for Rising Edge-based parity detection or Register 0x04[3] for Falling Edge-based parity. The status of IRQ can be measured via Register 0x06[2] or 0x06[3] or by using the IRQ pin. If using the IRQ pin and more than one IRQ is enabled, the user must check Register 0x06[3:2] when an IRQ event occurs to determine whether the IRQ was

caused by a parity error. The IRQ can also be cleared by writing a 1 to Register 0x06[2] or 0x06[3]

The PARITY bit feature can also be used to validate the interface timing. As described above, the host would provide a PARITY bit with the data samples as well as configure the AD9119/AD9129 to generate an IRQ. The user can then sweep the sampling instance of the AD9119/AD9129's input registers to determine at what point a sampling errors occur. The sampling instance can be varied in discrete increments by offsetting the nominal DLL phase shift value of 90° via SPI Reg 0x0A[3:0]. The equation below defines the phase offset relationship.

Phase Offset= $90° \pm n*11.25°$, $|n| < 8$

DIGITAL DATA PATH DESCRIPTION

A more detailed diagram of the AD9119/AD9129's digital data path is shown in Figure 136. The 22-bit/28-bit data path with internal Double Data Rate (DDR) clocking interfaces with the dual 11-bit/14-bit input data ports. Since two 11-bit/14-bit samples are captured on each clock edge of DCI, four consecutive samples are captured per DCI clock cycle. Samples captured on the *rising* edge of DCI propagate through the upper section at a rate of DACCLK/2 (DDR) while those captured on the *falling* edge propagate through the lower section.

After the input data has been captured, the data is passed through a logic block that monitors and/or determines the signal integrity of the high-speed digital data interface. The optional PARITY check is used to continuously monitor the digital interface on a sample per sample basis while the sample error detection (SED) can be used to validate the input data interface for system debug/test purposes. Note, FRAME and PARITY signals share the same pin assignment since FRAME is typically used during system initialization (for FIFO synchronization purposes) while PARITY is used in normal operation.

FIFO Description

The next functional block in the data path is a set of four FIFO's that are eight-registers deep. The dual port data is clocked into the FIFOs on both the rising and the falling edge of the DCI signal. The FIFO acts as a buffer that absorbs timing variations between the data source and DAC, such as the clock-to-data variation of an FPGA or ASIC. For the greatest timing margin, the FIFO level should be maintained near half full (i.e. a difference of four between the write and read pointers). The value of the write pointer determines the FIFO register into which the input data is written and the value of the read pointer determines the register from which data is read and fed into the data assembler. Write and read pointers, respectively, are updated every time new data is loaded and removed from the FIFO.

Valid data is transmitted through the FIFO as long as the FIFO does not overflow or become empty. Note that an over-flow or empty condition of the FIFO is the same as the write pointer and read pointer being equal. When both pointers are equal, an attempt is made to read and write a single FIFO register simultaneously. This simultaneous register access leads to unreliable data transfer through the FIFO and must be avoided by ensuring that data is written to the FIFO at the same rate that data is read from the FIFO, keeping the data level in the FIFO constant. This condition must be met by ensuring that DCI is equal to *DACCLK*/4 (or equivalently, DCO).

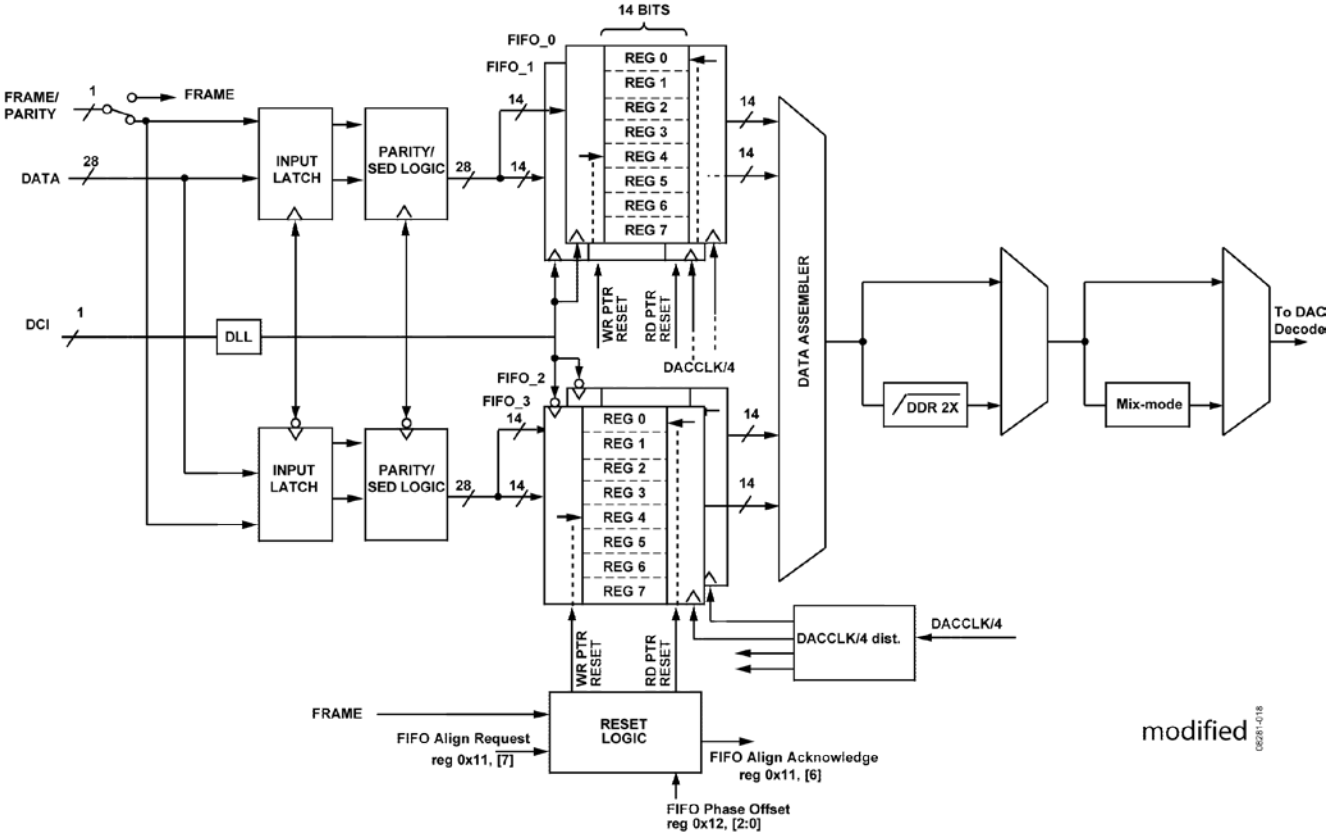


Figure 136. Digital Data Path of AD9119/AD9129

Resetting the FIFO Data Level

FIFO initialization is required to ensure a four sample spacing and a deterministic pipeline latency. If the clocks are running at power-up, the FIFO will initialize to 50% full.

To maximize the timing margin between the DCI input and the internal DAC data rate clock, the FIFO data level should be initialized prior to beginning data transmission. The value of the FIFO data level can be initialized in three ways: by resetting the device, by strobing the FRAME input, and via a write sequence to the serial port. The two preferred methods are use of the FRAME signal and via a write sequence to the serial port. Before initializing the FIFO data level, the LVDS DLL and the DAC clock PLL must be locked.

The FRAME input can be used to initialize the FIFO data level value. First, set up the FRAME pins for FRAME mode (Reg 0x07[1:0] = 2). Then, assert the FRAME signal high for at least one DCI clock cycle. When FRAME is asserted in this manner, the write pointer is set to 4 (by default or to the FIFO start level (Register 0x12, Bits[2:0])) the next time the read pointer becomes 0 (see Figure 137).

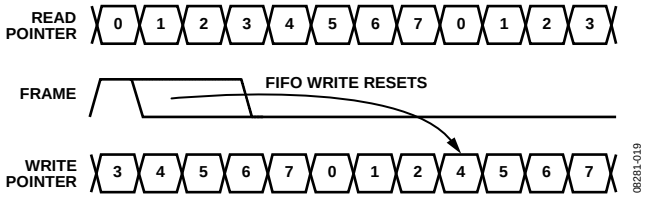


Figure 137. Timing of the FRAME Input vs. Write Pointer Value

To initialize the FIFO data level through the serial port, Bit 7 of Register 0x11 should be toggled from 0 to 1. When the write to the register is complete, the FIFO data level is initialized.

The recommended procedure for a serial port FIFO data level initialization is as follows:

- Request FIFO level reset by setting Register 0x11, Bit 7 to 1.
- Verify the part acknowledges the request by ensuring Register 0x11, Bit 6 is 1.
- Remove the request by setting Register 0x11, Bit 7 to 0.
- Verify the part drops the acknowledge signal by ensuring Register 0x11, Bit 6 is 0.

Monitoring the FIFO Status

The FIFO initialization and status can be read from Register 0x17. This register provides information on the FIFO initialization method, and whether the initialization was successful. Two status bits in the FIFO Status Register 0x17[7:6], FIFO Warn 1 and FIFO Warn 2, are available for monitoring the FIFO level. These flags indicate that the FIFO is close to emptying (FIFO level is 1) or approaching the empty state (FIFO level is 2). This is an indication that data may soon be corrupted, and action should be taken.

The FIFO data levels can be read from Registers 0x13 through 0x16 at any time. The serial port reported FIFO data level is denoted as a 7-bit thermometer code of the write counter state relative to the absolute read counter being at 0. The optimum FIFO data level of 4 is therefore reported as a value of 0001111 in the status register. It should be noted that, depending on the timing relationship between DCI and the main DACCLK, the FIFO level value can be off by ±1 count. Therefore, it is important to keep the difference between the read and write pointers to at least 2.

Multi-DAC Synchronization

Synchronization of multiple AD9119/AD9129's implies that each of the DAC's outputs are time-aligned to the same phase when all devices are fed with the same data pattern (along with DCI) at the same instance of time. FIFO initialization ensures that the initial pipeline latency in the FIFO is set to 4-samples and remains at this level assuming no process, voltage, or temperaturevariations between the host and AD9119/AD9129 clock domains. Figure 138 shows an example of two AD9119/AD9129 devices synchronized to the same host (i.e. FPGA, ASIC). Note, synchronization to a single host IC ensures minimum data and DCI time skew between devices when the same resources are used to generate these output signals.

Even after FIFO initialization, a phase ambiguity still exists between each device's read pointers since each device's read counter powers-up in an arbitrary state; hence the exact instance when their respective write pointer is set to 4 after FRAME is asserted also remains ambiguous. Referring to Figure 137, it is possible that one device's read pointer reaches its 0 count several clock cycles before another device.

Synchronization to within a data sample requires insight into the difference between the master and slave devices' read pointer as well as the ability to vary the delay of the slave device(s) within the host to compensate for initial offsets between devices. It is possible to calculate how many data samples the slave device(s) is offset from the master device for the following reasons:

- Pipeline delay of each device is the same after FIFO initialization.
- Each device's read counter is derived from the same phase aligned DACCLK source.
- The state of each device's read counters are sampled at the same instance in time via FRAME signal
- The readback value (Reg 0x12[6:4]) is normalized to a data sample (i.e. DACCLK period).

By calculating the difference between the master and slave devices' read pointer settings, one can advance or delay the slave device's data stream within the FPGA. Since this difference can

be up to +/-4 data samples, the FPGA must provide this adjustment range for DAC synchronization alone. Note, additional range must be added to compensate for any other system delay variation.

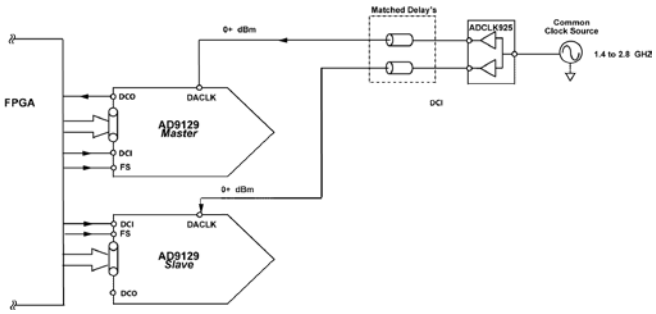


Figure 138. Example of Synchronization of two DACs to one FPGA.

In addition to synchronizing to the data sample level, the AD9119/AD9129 has a facility to enable synchronization to the DACCLK level. Figure 139 shows the concept. A 1.8V CMOS output pin, Sync, can be used to provide a DACCLK/8 signal. Using the Sync output from each DAC, enabled by Register 0x1A[4] = 1, the user can create a simple phase detector with an external XOR gate. By adjusting the delay line in the DACCLK PLL (incrementing or decrementing by one DAC CLK cycle with each write to Register 0x1A[7] or [6], respectively), the user can align the DACCLKs inside the two DACs to within +/-2 DAC clock cycles, when errors from the external phase detector, lowpass filter, and delay differences are taken into account. The existing phase position can be read from bits [2:0].

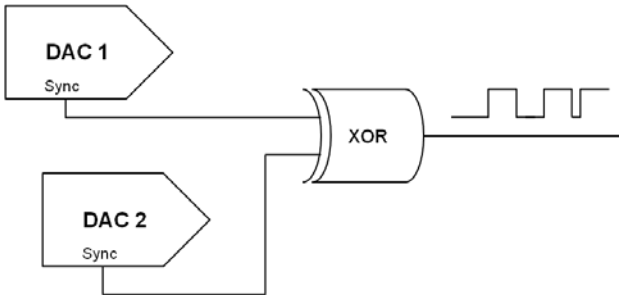
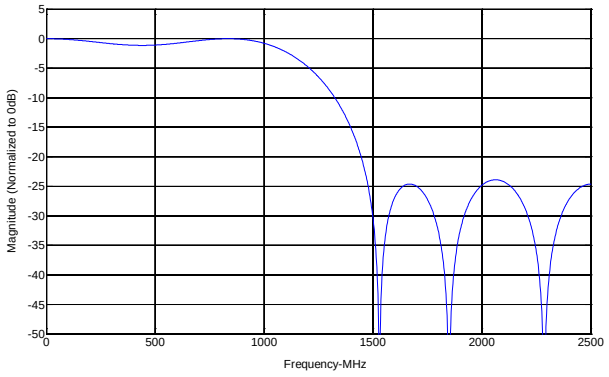


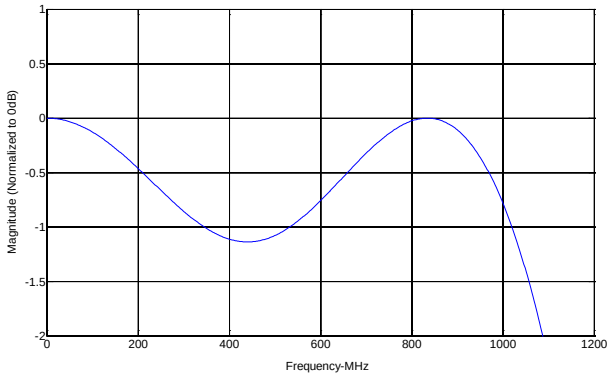
Figure 139. Example of synchronization of two DACs to +/-2 DACCLK accuracy

Data Assembler and Signal Processing Modes

The Data Assembler reconstructs the original sample sequence. It consists of a 4:1 multiplexer operating at F_{DACCLK}. Each of the four FIFOs provides a sample that is now referenced to the AD9119/AD9129's internal clock domain, F_{DACCLK}. The reconstructed sample sequence can be directed to the DAC's decode logic or undergo additional signal processing. In 2x interpolation mode, a FIR filter is used to generate a new data sample that is inserted between each sample such that it can update the DAC decode logic on the *falling* edge of DACCLK. In mix-mode, the complement of each data sample is generated and inserted after it such that it also updates the DAC in a similar manner. The 2x interpolator can be used with mix-mode enabled.

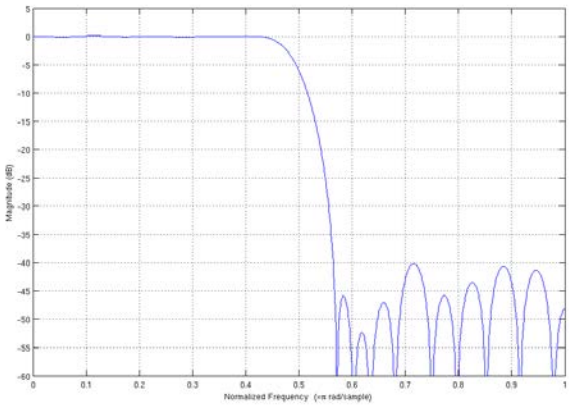


a)

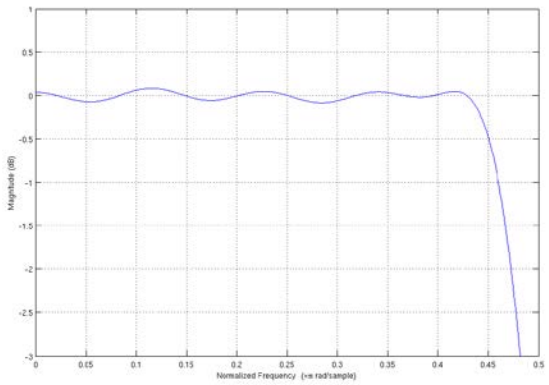


b)

Figure 140. Plots of the FIR25 2x interpolator filter shows a) the complete frequency response along with b) the passband ripple. f_{DAC} = 2.5 GHz



a)



b)

Figure 141. Plots of the FIR40 2x interpolator filter show a) the complete frequency response along with b) the passband ripple.

2x Digital Filter

The AD9119/AD9129 includes a bypassable 2x halfband interpolation filter to help simplify the analog reconstruction filter. The filter has the potential benefit of minimizing the impact of folded back harmonics in the desired baseband region. The filter operates in a dual-edge clocking mode where it generates a new interpolated sample value for every alternate DACCLK edge. This effectively increases the DAC update rate to 2*f_{DACCLK} with the DAC's sinc response null moving from f_{DACCLK} to 2*f_{DACCLK}.

There are two different filters, FIR25 and FIR40, that can be chosen using register bit 0x18[5] when the 2x interpolator is enabled with register bit 0x18[7].

The FIR25 half band filter provides 25 dB of stopband rejection. Its response is shown in Figure 140. Coefficients were optimized for practical implementation purposes with the notion that the +/-0.5 dB pass band ripple effects on a multi-carrier application (e.g. DOCSIS) can be compensated by the digital host adjusting individual channel powers. Note, the worst case "tilt" across any 6 MHz channel is less than -0.05 dB.

The FIR40 half-band filter provides 40 dB of stopband rejection, and its response is shown in Figure 141. Coefficients were chosen to reduce passband ripple and increase out-of-band rejection for multi-carrier applications (e.g, DOCSIS). As a result, the frequency response has a flatter in-band response and a sharper transition region, and the trade-off is higher tap count leading to higher pipeline delay, and higher power consumption. The two filters are compared in Table 11.

Table 11. Features of the two 2x interpolator filters

Filter	Ripple (dB)	Atten (dB)	Power (mW)
FIR25	+/-0.5	25	150
FIR40	+/-0.1	40	450

A duty cycle restore circuit follows the DACCLK clock receiver to minimize impact of duty cycle errors on image rejection.

Pipeline Delay (Latency)

The AD9129's pipeline delay, or latency, will vary based on the configuration chosen, and can be calculated using the formula below.

Pipeline_total = Pipeline_delay + 2x_delay + Group_delay + FIFO_level

and the values in the below Table 12 can be used, depending on the mode of operation that is selected.

Table 12. Pipeline delay values for each block

Mode	Pipeline delay	Group Delay	Total Pipeline	Total delay
No 2x filter	74 f_{DAC} cycles	--	74 f_{DAC} cycles	74 f_{DAC} cycles
With FIR25	+43	+2	117 f_{DAC}s	119 f_{DAC}s
With FIR40	+67	+9	141 f_{DAC}s	150 f_{DAC}s

where

Pipeline_delay is the time from DAC code latched until the DAC output begins to move

Group delay is the time for the max amplitude pulse to reach the DAC output as compared to the first time the output moves

No 2x filter is the base pipeline delay including data interface, analog circuitry (6 cycles) and data FIFO at half full/position 3

FIR25 is the 2x interpolator with 25 dB of out-of-band rejection

FIR40 is the 2x interpolator with 40 d B of out-of-band rejection

Note that the values for pipeline delay apply both in Normal mode as well as Mix-mode™. Once the total delay through the digital blocks is calculated, add the FIFO level to that delay to find the total pipeline delay. Note that the pipeline delay can be considered fixed, with the only ambiguity being the FIFO state. The FIFO state can be initialized as part of the startup sequence to ensure a four sample spacing and therefore a fixed pipeline delay, or deterministic latency. (See "Resetting the FIFO Data Level" for more information.)

Power Up Time

The AD9119/AD9129 has a power down register (reg 0x01) that enables the user to power down various portions of the DAC. The power up time for several use cases is shown in Table 13. The recommended way to power up the AD9119/AD9129 is to

power up all parts of the circuit with Iref disabled (reg 0x01[6] = 1), and then enable Iref by programming reg 0x01[6] = 0.

Table 13. Power up times for several usage cases

State	Register State	Time (usec)
Power Up	0x01 = 0xEF --> 0x01 = 0x08	250
Clock Path Up	0x01 = 0x0C--> 0x01 = 0x08	220
Wake Up	0x01 = 0x48--> 0x01 = 0x08	2

INTERRUPT REQUESTS

The AD9119/AD9129 can provide the host processor an interrupt request output signal (IRQ) that one or more of the following events occurred:

- One of the AD9119/AD9129's clock controllers has established or lost lock.
- PARITY error has occurred.
- Sample Error Detection status or result is ready
- The FIFO is nearing an overwrite status

The IRQ output signal is an *active low* output signal available on pin IRQ (H2). If used, its output should be connected via a 10 kΩ pull-up resistor to VDD.

Each IRQ is enabled by setting the enable bits in Registers 0x03 and 0x04 which have the same bit mapping as the IRQ status bits in Registers 0x05 and 0x06. If an interrupt bit is not enabled, a read request of that bit will show a direct readback of the source's current state. Thus, a read request of either register will show the current state of all 8 interrupts in that register, regardless of whether each individual bit is actually enabled to generate an interrupt. When an interrupt bit is enabled, it will capture a rising edge of the interrupt source and hold it, even if the source subsequently returns to its zero state. It is possible, for example, for the x_LCK_IRQ and x_LST_IRQ status bits to be set when a controller temporarily lost lock but was able to reestablish lock before the IRQ was serviced by the host. In this case, the host should validate the *present* status of the suspect block by reading back its current status bits. Based on the status of these bits, the host can take appropriate action, if required. The IRQ pin will only respond to those interrupts that have been enabled. To clear an IRQ, it is necessary to write a 1 to the bit in Register 0x05 or 0x06 that caused the interrupt. A detailed diagram of the interrupt circuitry is shown in Figure 142.

Table 14. INTERRUPT REQUEST REGISTERS

Address (Hex)	Bit	Description
0x05	7	Indicates that the FIFO is within 2 slots of overwrite
	6	Indicates that the FIFO is within 1 slots of overwrite
	5	Indicates acknowledgement from SpiFrmReq-->1
	4	RESERVED
	3	Indicates that the DataReceiver is close to coming unlocked and action is needed.
	2	Indicates that DataReceiver is now locked
	1	Indicates that the Retimer PLL is no longer locked
	0	Indicates that the Retimer PLL is now locked
0x06	7	Indicates that all BIST vectors were processed
	6	Indicates that the AED logic has captured 8 valid samples
	5	Indicates that the AED logic has detected a mis-compare
	4	Indicates the SED FAIL interrupt; reporting that a mis-compare occurred
	3	Indicates a Parity fault due to data captured on the Falling Edge
	2	Indicates a Parity fault due to data captured on the Rising Edge
	1	RESERVED
	0	RESERVED

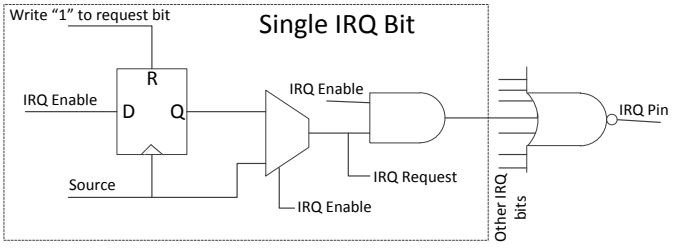


Figure 142. Interrupt Request Circuitry

It is also possible to use the IRQ during the AD9119/AD9129 initialization phase after power-up to determine when the Retimer PLL and Data Receiver controllers have achieved lock. For example, before enabling the Retimer PLL, the Retime_LCK_EN bit can be set and then the IRQ output signal can be monitored to determine when lock has been established before continuing in a similar manner with the Data Receiver controller. Clear the relevant LCK bit after locking before continuing to the next controller. Once all of the controllers are locked, set the "lost lock enable" bits (i.e. x_LST_EN) to continuously monitor the controllers for loss of lock.

INTERFACE TIMING VALIDATION

The AD9119/AD9129 provides on-chip sample error detection (SED) circuitry that simplifies verification of the input data interface. The SED compares the input data samples captured at the digital input pins with a set of comparison values. The comparison values are loaded into registers through the SPI port. Differences between the captured values and the comparison values are detected and stored. Options are available for customizing SED test sequencing and error handling.

SED OPERATION

The SED circuitry operates on a data set made up of four 11-bit/14-bit input words, denoted as I0R, I1R, I0F, and I1F. These represent data port 0 and 1 Rising Edge and Falling Edge data. (The AD9119/AD9129 uses both edges of the DCI clock to sample data on each input port.) To properly align the input samples, the data ports' rising edge data words (that is, I0R and I1R) are indicated by asserting the FRAME signal for a minimum of two complete input samples.

Figure 143 shows the input timing of the interface in word mode. The FRAME signal can be issued once at the start of the data transmission, or it can be asserted repeatedly at intervals coinciding with the I0R and I1R data-words.

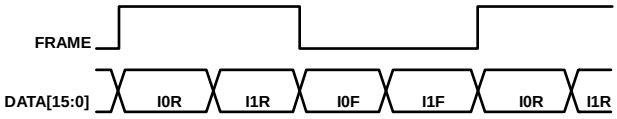


Figure 143. Timing Diagram of Extended FRAME Signal Required to Align Input Data for SED

The SED has three flag bits (Register 0x50, Bit 0, Bit 1, and Bit 2) that indicate the results of the input sample comparisons. The sample error detected bit (Register 0x50, Bit 0) is set when an error is detected and remains set until cleared. The SED also provides registers that indicate which input data bits experienced errors (Register 0x51 through Register 0x58). These bits are latched and indicate the accumulated errors detected until cleared.

The Autosample Error Detection (AED) mode is an autoclear mode that has two effects: it activates the compare fail bit and the compare pass bit (Register 0x50, Bit 1 and Bit 2) and changes the behavior of Register 0x51 through Register 0x58. The compare pass bit sets if the last comparison indicated the sample was error free. The compare fail bit sets if an error is detected. The compare fail bit is automatically cleared by the reception of eight consecutive error-free comparisons. When autoclear mode is enabled, Register 0x51 through Register 0x58 accumulate errors as previously described but reset to all 0s after eight consecutive error-free sample comparisons are made.

The sample error, compare pass, and compare fail flags can be configured to trigger an $\overline{\text{IRQ}}$ when active, if desired. This is done by enabling the appropriate bits in the event flag register (Register 0x06, bits 4, 5, and 6).

SED EXAMPLE

Normal Operation

The following example illustrates the SED configuration for continuously monitoring the input data and assertion of an $\overline{\text{IRQ}}$ when a single error is detected.

1. Write to the following registers to enable the SED and load the comparison values.
   Register 0x50 → 0x80
   Register 0x50 → 0xC0
   Register 0x50 → 0x80
   Register 0x51 → I0R[7:0]
   Register 0x52 → I0R[13:8]
   Register 0x53 → I1R[7:0]
   Register 0x54 → I1R[13:8]
   Register 0x55 → I0F[7:0]
   Register 0x56 → I0F[13:8]
   Register 0x57 → I1F[7:0]
   Register 0x58 → I1F[13:8]
   Comparison values can be chosen arbitrarily; however, choosing values that require frequent bit toggling provides the most robust test.
2. Enable the SED error detect flag to assert the $\overline{\text{IRQ}}$ pin.
   Register 0x04 → 0x10
3. Begin transmitting the input data pattern.

If $\overline{\text{IRQ}}$ is asserted, read Register 0x50 and Register 0x51 through Register 0x58 to verify that a SED error was detected and determine which input bits were in error. The bits in Register 0x51 through Register 0x58 are latched. This means the bits indicate any errors that occurred on those bits throughout the test and not just the errors that caused the error detected flag to be set.

ANALOG INTERFACE CONSIDERATIONS

ANALOG MODES OF OPERATION

The AD9119/AD9129 uses the quad-switch architecture shown in Figure 144. Only one pair of switches is enabled during a half-clock cycle thus requiring each pair to be clocked on alternative clock edges. A key benefit of the quad-switch architecture is that it masks the code-dependent glitches which occur in the conventional two-switch DAC architecture.

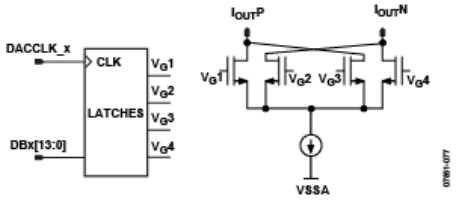


Figure 144. AD9119/AD9129 Quad-Switch Architecture

In the two-switch architecture, when a switch transition occurs and D_1 and D_2 are in different states, a glitch occurs. But, if D_1 and D_2 happen to be at the same state, the switch transitions, and no glitches occur. This code-dependent glitching causes an increased amount of distortion in the DAC. In the quad-switch architecture (no matter what the codes are), there are always two switches transitioning at each half clock cycle, thus eliminating the code-dependent glitches but, in the process, creating a constant glitch at 2 × DACCLK. For this reason, a significant clock spur at 2 x F_{DACCLK} will be evident in the DAC output spectrum.

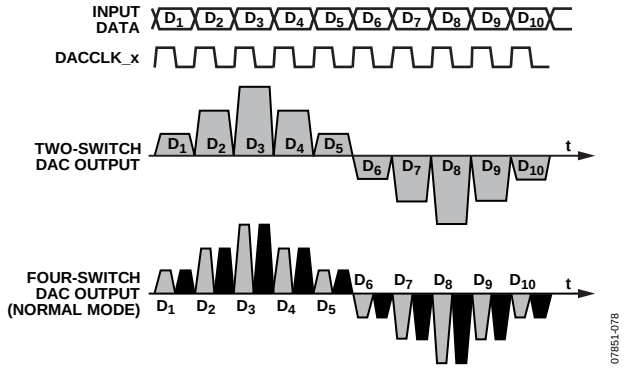


Figure 145. Two-Switch and Quad-Switch DAC Waveforms

As a consequence of the quad-switch architecture enabling updates on each *half* clock cycle, it is possible to operate that DAC core at *twice* the DACCLK rate if new data samples are latched into the DAC core on both the *rising* and *falling* edge of the DACCLK. This notion serves as the basis when operating the AD9119/AD9129 in either mix-mode or with the 2x interpolation filter enabled. In each case, the DAC core is presented with new data samples on each clock edge, albeit in mix-mode, the *falling* edge sample is simply the complement of the *rising* edge sample value.

In the mix-mode, the output is effectively chopped at the DAC sample rate. This has the effect of reducing the power of the fundamental signal while increasing the power of the images centered around the DAC sample rate, thus improving the dynamic range of these images.

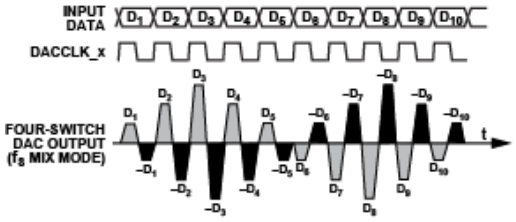


Figure 146. Mix-Mode Waveform

This ability to change modes provides the user the flexibility to place a carrier anywhere in the first three Nyquist zones, depending on the operating mode selected. Switching between baseband and mix-mode reshapes the sinc roll-off inherent at the DAC output. In baseband mode, the sinc null appears at F_{DACCLK} since the same sample latched on the *rising* clock edge is also latched again on the *falling* clock edge hence resulting in the same ubiquitous sinc response of a traditional DAC. In mix-mode, the *complement* sample of the *rising* edge is latched on the *falling* edge hence pushing the sinc null to 2 x F_{DACCLK}. Figure 147 shows the ideal frequency response of both modes with the sinc roll-off included.

The quad-switch can be SPI configured (Reg 0x19, bit[0]) to operate in either baseband (0)or mix-mode (1).

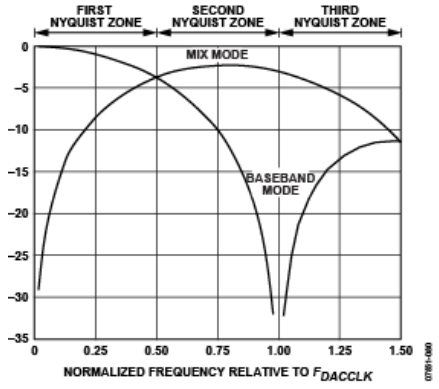


Figure 147. Sinc Roll-Off for Baseband and Mix-Mode Operation.

CLOCK INPUT

The AD9119/AD9129 contains a low jitter differential clock receiver capable of interfacing directly to a differential or single-ended clock source. Since the input is self-biased to a nominal mid-supply voltage of 1.25 V with a nominal impedance of 10 Kohm//2 pF, it is recommended that the clock source be AC coupled to the DACCLK input pins with an external differential load of 100 ohms. While the nominal differential input span is 1 Vpp, the clock receiver can operate with a span ranging from 250 mVpp to 2.0 Vpp.

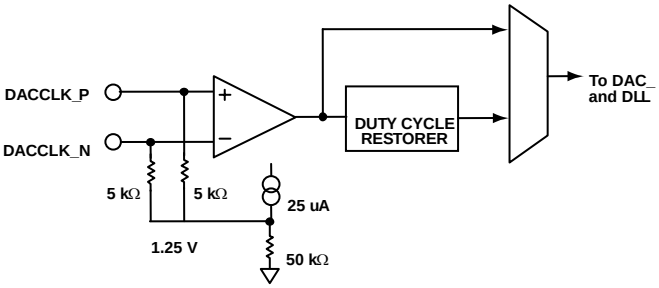


Figure 148. AD9119/AD9129 Clock Input

The quality of the clock source as well as its interface to the AD9119/AD9129's clock input directly impacts its AC performance. The phase noise and spur characteristics of the clock source should be selected to meet the target applications requirements. Phase noise and spurs at a given frequency offset on the clock source get directly translated to the output signal. It can be shown that the phase noise characteristics of a reconstructed output sine wave is related to the clock source by $20*\log10(F_{OUT}/F_{CLK})$ when the DAC clock path contribution is negligible. (The wideband noise is not dominated by the DAC's thermal and quantization noise.)

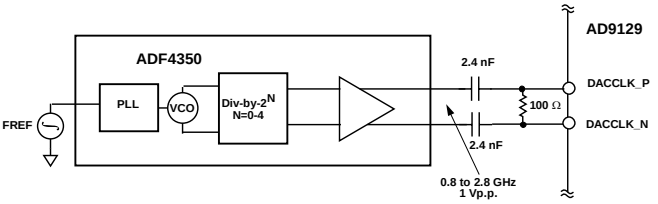


Figure 149. Possible signal chain for AD9119/AD9129 DACCLK input

Figure 149 shows a clock source based on the ADF4350 low phase noise/jitter PLL. The ADF4350 can provide output frequencies from 140 MHz up to 4.4 GHz with jitter as low as 0.5 psec rms. Its squared-up output level can be varied from -4 to +5 dBm allowing further optimization of the clock drive level.

A clock control register exists at address 0x30. This register can be used to enable automatic duty cycle correction (bit 1), enable zero crossing control (bit 6), and set the zero-crossing point (bits [5:2]). Recommended settings for this register are given in the recommended start-up sequence (see Startup Sequence).

The input impedance of the AD9119/AD9129 DACCLK input is shown in Figure 150.

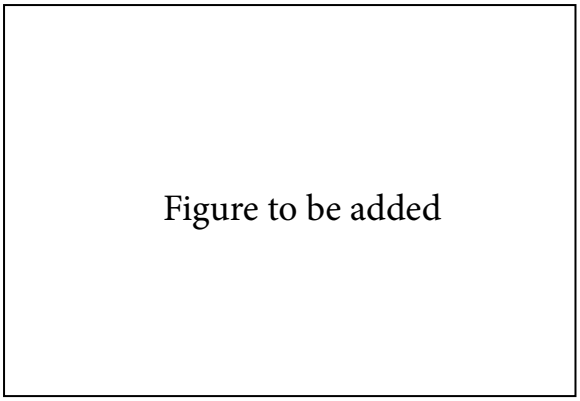


Figure 150. Smith chart of AD9119/AD9129 DACCLK input (S11)

PLL

The DACCLK input goes to a high frequency PLL to ensure robust locking of the DAC sample clock to the input clock. The PLL is enabled by default, so upon power up the PLL will lock. The PLL (or DAC Clock Retimer) control registers are located at 0x33 and 0x34. Register 0x33 enables the user to set the phase detector phase offset level ([7:4]), clear the PLL Lost Lock status bit (bit 3), choose the PLL divider for optimum performance (bit 2), and choose the phase detector mode (bits [1:0]). These settings are determined during product characterization and are given in the recommended start-up sequence (see Startup Sequence). It is not normally necessary to change these values, nor is the product characterization data valid on any settings other than the recommended ones. Register 0x34 is used to reset the PLL, should that become necessary.

At DACCLK = 2.8 GSPS, the lock time is about 10 µs. In most situations, no action need be taken with the PLL. If the DACCLK is changed, and especially if it is changed multiple times as in a frequency hopping application, a phase slip or glitch may be caused by the change in frequency and it may become necessary to reset the PLL. This can be checked by reading the PLL Retimer Lost Lock bit (Reg 0x35[6]). If that is the case, the PLL Reset bit should be toggled by programming Reg 0x34[3] HIGH then LOW. The PLL Retimer Lost Lock bit should also be cleared by writing a 0 to Reg 0x35[6]. Lock of the PLL can be verified by reading the PLL Lock bit at Reg 0x35[7]. It is possible to use the IRQ registers to set an interrupt for these events. See the Interrupt Requests section for more details.

VOLTAGE REFERENCE

The AD9119/AD9129 output current is set by a combination of digital control bits and the I250U reference current, as shown in Figure 151.

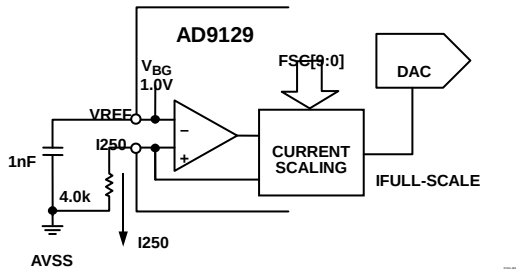


Figure 151. Voltage Reference Circuit

The reference current is obtained by forcing the band gap voltage across an external 4.0 kΩ resistor from I250U (Pin A1) to ground. The 1.0 V nominal band gap voltage (VREF) generates a 250 μA reference current in the 4.0 kΩ resistor. Note the following constraints when configuring the voltage reference circuit:

1. Both the 4.0 kΩ resistor and 1 nF bypass capacitor are required for proper operation.
2. Adjusting the DAC's output full-scale current, I_{OUTFS} , from its default setting of 20 mA should be performed digitally.
3. The AD9119/AD9129 is not a multiplying DAC. Modulating the reference current, I250U, with an AC signal is not supported.
4. The bandgap voltage appearing at the VREF pin must be buffered for use with an external circuitry since its output impedance is approximately 7.5 kΩ .
5. An external reference can be used to overdrive the internal reference by connecting it to the VREF pin.

As mentioned, the I_{OUTFS} can be adjusted digitally over a 9.5 to 34.4 mA range by FSC[9:0] (Register 0x20[7:0] and Register 0x21[1:0]). The following equation relates I_{OUTFS} to the FSC[9:0] register which can be set from 0 to 1023.

$$I_{OUTFS} = 24.35 \times FSC[9:0] /1000 + 9.47 \quad (1)$$

Note, the default value of 0x200 generates 21.937 mA full scale, but most of the characterization presented in this datasheet uses 33 mA (unless noted otherwise).

ANALOG OUTPUTS

Equivalent DAC Output and Transfer Function

The AD9119/AD9129 provides complementary current outputs, IOUTP and IOUTN, that sink current from an external load referenced to the 1.8 V VDDA supply. Figure 152 shows an equivalent output circuit for the DAC. Compared to most current output DAC's of this type, the AD9119/AD9129's outputs exhibits a slight offset current (i.e. $I_{OUTFS}/17$) and the peak differential AC current is slightly below $I_{OUTFS}/2$ (i.e. 8/17* I_{OUTFS}).

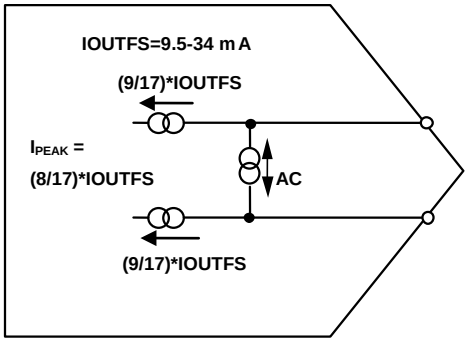


Figure 152. Equivalent DAC output circuit

Referring to Figure 152, it can be modeled as a pair of DC current sources that source a current of $9/17*I_{OUTFS}$ to each output. A differential AC current source, $I_{PEAK,}$ is used to model the signal (i.e. digital code) dependent nature of the DAC output. The polarity and signal dependency of this AC current source is related to the digital code by the following equation:

$$F(code)=(DACCODE-8192)/8192 \quad (2)$$

$$-1 \leq F(code) <1 \quad (3)$$

where DAC CODE = 0 to 16,383 (decimal).

Since I_{PEAK} can swing +/-(8/17)* I_{OUTFS} , the output currents measured at IOUTP and IOUTN can span from $I_{OUTFS}/17$ to I_{OUTFS}. However, since the AC signal dependent current component is complementary, the sum of the two outputs will always be constant (i.e. $IOUTP + IOUTN = (18/17)* I_{OUTFS}$).

The code-dependent current measured at the IOUTP (and IOUTN) output are as follows:

$$IOUTP=9/17*I_{OUTFS}+8/17*I_{OUTFS}*F(code)] \quad (3)$$

$$IOUTN=9/17*I_{OUTFS}-8/17*I_{OUTFS}*F(code)] \quad (4)$$

Figure 153 shows the IOUTP vs DACCODE transfer function when I_{OUTFS} is set to 19.65 mA.

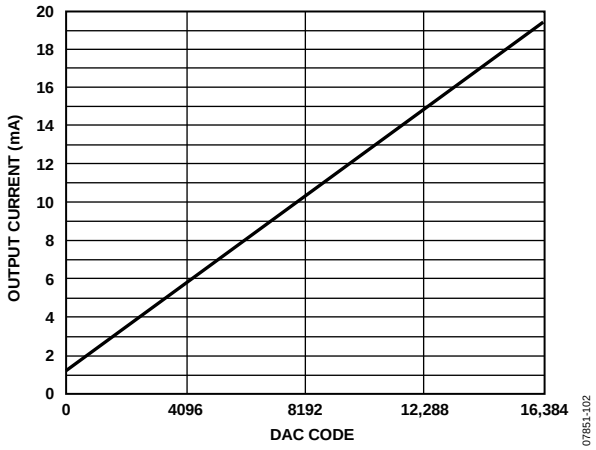


Figure 153. Gain Curve for FSC[9:0] = 512, DAC OFFSET = 1.228 mA

Peak DAC Output Power Capability

The maximum peak power capability of a differential current output DAC is dependent on its peak differential AC current, $I_{PEAK,}$ and the equivalent load resistance it sees. In the case of a 1:1 balun with 50 ohm source termination, the equivalent load seen by the DAC's AC current source is 25 ohms. If the AD9119/AD9129 is programmed for an I_{OUTFS}=20 mA, its peak AC current is 9.375 mA and its peak power delivered to the equivalent load is 2.2 mW (i.e. $P=I^2R$) . Since the source and load resistance seen by the 1:1 balun are equal, then this power will be shared equally. Hence the output load will receive 1.1 mW, or 0.4 dBm peak power.

To calculate the rms power delivered to the load, consider the following:

1) Peak-to-Rms of digital waveform
2) Any digital back-off from digital full-scale.
3) DAC's Sinc response and non-ideal losses in external network.

For example, a reconstructed sine wave with no digital back-off will ideally measure -2.6 dBm since it has a peak-to-rms ratio of 3 dB. If one includes a typical balun loss of 0.4 dBm, one would expect to measure -3 dBm of actual power in the region where the DAC's Sinc response has negligible influence. Increasing the output power is best accomplished by increasing I_{OUTFS} .

Output Stage Configuration

The AD9119/AD9129 is intended to serve high dynamic range applications that require wide signal reconstruction bandwidth (i.e. DOCSIS CMTS) and/or high IF/RF signal generation. Optimum AC performance can only be realized if the DAC's output is configured for differential (i.e. balanced) operation with its output common-mode voltage biased to a stable, low noise 1.8 V nominal analog supply (VDDA). The ADP150 LDO can be used to generate a clean 1.8 V supply.

The output network used to interface to the DAC should provide a near 0 ohm DC bias path to VDDA. Any imbalance in the output impedance over frequency between the IOUTP and IOUTN pins will degrade the distortion performance (mostly even order) and noise performance. Component selection and layout are critical in realizing the AD9119/AD9129's performance potential.

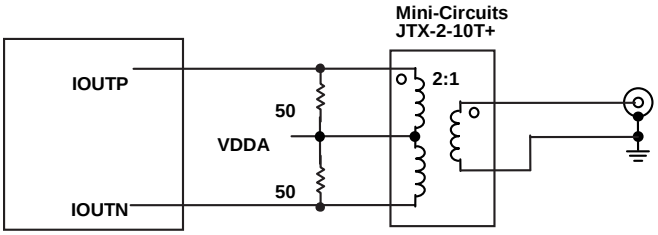


Figure 154. Recommended transformer for Wideband applications with upper bandwidth's up to 2.2 GHz

Most applications requiring balanced-to-unbalanced conversion from 10 MHz-1 GHz can take advantage of Mini-Circuits JTX series of transformers that offer both 2:1 and 1:1 impedance ratios. Figure 154 shows the AD9119/AD9129 interfacing to the JTX-2-10T transformer. This transformer provides excellent amplitude/phase balance (i.e. <1 dB/1°) up to 1 GHz while providing a 0 ohm DC bias path to VDDA. If filtering of the DAC's images and clock components is required, applying an analog LC filter on the single-ended side has the advantage of preserving the transformer's balance.

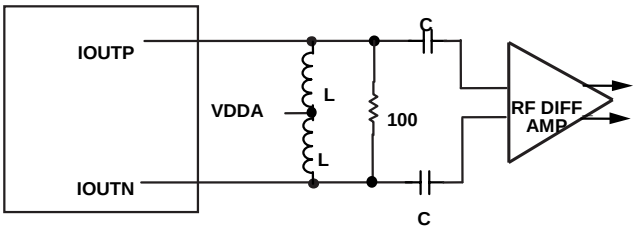


Figure 155. Interfacing the DAC output to self-biased differential gain stage

Figure 155 shows an interface that can be considered when interfacing the DAC output to a self-biased differential gain block. The inductors shown serve as RF Chokes (L) that provide the DC bias path to AGND. Its value, along with the DC blocking capacitors, will determine the lower cut-off frequency of the composite pass band response. (The DC blocking capacitors form a high pass response with the input resistance of the RF differential gain stage.)

Many RF differential amplifiers actually consist of two single-ended amplifiers with matched gain hence providing no common-mode rejection while possibly degrading the balance due to poor matching characteristics. Also, depending on the component tolerances, differential LC filters can further degrade the balance in a differential signal path. In both cases,

the use of a balun could be advantageous in rejecting the common-mode distortion and noise components from the RF DAC prior to filtering or further amplification.

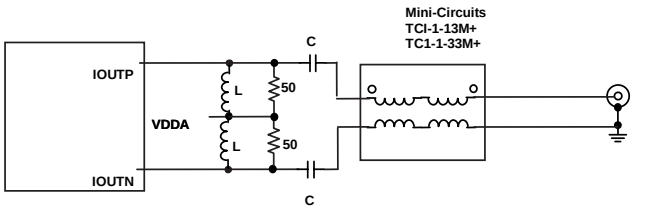


Figure 156. Recommended Mix-Mode configuration offering extended RF bandwidth using TC1-1-43A+ balun

Applications operating the AD9119/AD9129 in mix-mode with output frequencies extending beyond 2.2 GHz may want to consider the circuit shown in Figure 156. The circuit in Figure 156 uses a wideband balun (i.e. -3 dB @ 4.0 GHz) with a similar configuration as Figure 154 to provide a DC bias path for the DAC outputs. This circuit was implemented on an evaluation board and the frequency response was measured to compare it with the ideal curve in Figure 147. The result is shown in Figure 157.

Figure to be added

Figure 157. Measured vs. Ideal Response for AD9129 (f_{DAC} = 2600 MHz)

STARTUP SEQUENCE

A small number of steps are necessary to program the AD9119/AD9129 to the proper operating state after powering up the device. This sequence is given below, along with comments explaining the purpose of each step.

Register	Value	Comment
0x00	0x00	4-wire spi, msb first packing, short addressing mode
0x30	0x5C	Enable cross control, cross, cross location = 7, duty cycle correction off
0x01	0x68	Bias powerdown
0x34	0x9D or 0x5D	Set PLL mode for Normal or 2x mode: Normal mode = 0x9D Interpolator on = 0x5D
0x01	0x48	Enable bias
0x33	0x13	Initialize PLL to phase step = 1
0x33	0xF8 or 0xD8	Select PFD, set PLL phase step, keep PLL Lost bit cleared. Phase step is Normal mode = 0xF8 Interpolator on = 0xD8
0x33	0xF0 or 0xD0	De-assert the PLL Lost bit, keeping the phase step. Normal mode = 0xF0 Interpolator on = 0xD0
0x0C	0x63	Enable DCO
0x0A	0x40	Set DLL phase to 0, turn on duty cycle correction
0x0D	0x06	Set duty correction bandwidth to lowest.
0x0A	0xC0	Enable DLL
0x11	0x01	Enable FIFO phase reporting
0x18	0xm0	Select Data mode, filter mode to set value of m: Example: 0x40, unsigned data, interpolator off
0x20	0xC6	Set Full Scale Current (FSC) to 33 mA
0x21	0x03	Finish setting FSC
0x30	0x46	Enable cross control, cross location = 1, enable duty cycle correction
0x11	0x80	Assert FIFO reset
0x11	0x80	De-assert FIFO reset
0x01	0x00	Enable Iref (DAC output)

OUTLINE DIMENSIONS

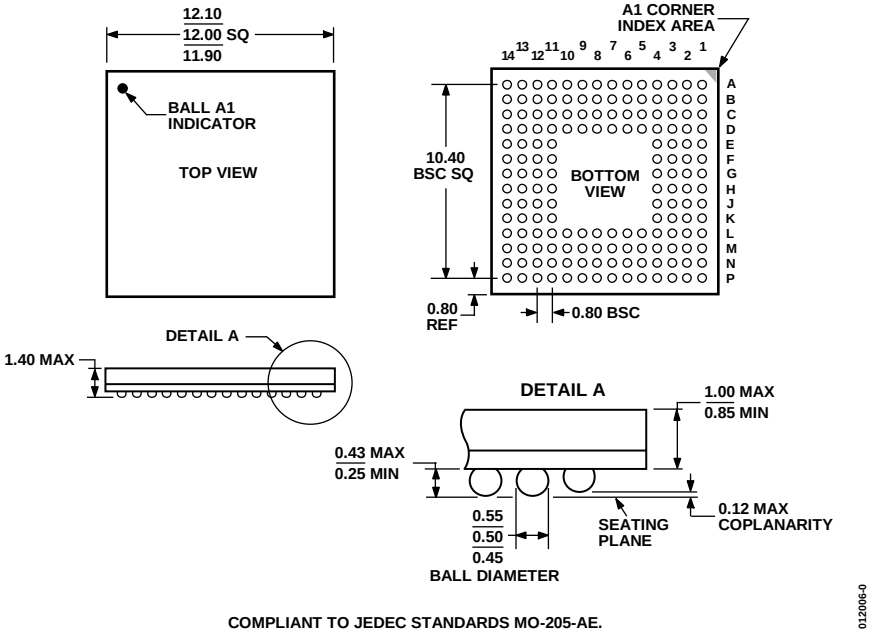


Figure 158. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-160-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9119BBCZ[1]	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9119BBCZRL[1]	−40°C to +85°C	160- Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9119-EBZ[1]		Evaluation Board for Normal Mode Evaluation	
AD9119-MIX-EBZ		Evaluation Board for Mix-mode Evaluation	
AD9129BBCZ[1]	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9129BBCZRL[1]	−40°C to +85°C	160- Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9129BBC	−40°C to +85°C	160- Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9129BBCRL	−40°C to +85°C	160- Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9129-EBZ[1]		Evaluation Board for Normal Mode Evaluation	
AD9129-MIX-EBZ		Evaluation Board for Mix-mode Evaluation	
AD9129-CBLTX-EBZ		Evaluation Board for Cable Transmitter Evaluation	

[1] Z = RoHs Compliant Part.

APPENDIX A

DEVICE CONFIGURATION AND REGISTER MAP DESCRIPTION

Table 15. Device Configuration Register Map

REGISTER NAME	ADDRESS		TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEF
MODE	**0X00**	0	R/W	SDIO_DIR	LSB/MSB	SOFTRESET	SHORT/LONG	*MIRROR FOR SAFETY BIT[3]=SHORT/LONG, BIT[2]=SOFTRESET, BIT[1]=LSB/MSB, BIT[0]=SDIO_DIR*				0X81
POWER DOWN	**0X01**	1	R/W	BG_PD	IREF_PD	BIAS_PD	CURGEN_PD	1	CLKPATH_PD	RETIMER PD	DATARCVR PD	0X48
IRQ ENABLE 0	**0X03**	3	R/W	FIFO_WARN2	FIFO_WARN1	SPIFRMACK		DLL_WARN	DLL_LOCK	RETIME LOST	RETIME LOCK	0X00
IRQ ENABLE 1	**0X04**	4	R/W	PBIST DONE	AED PASS	AED FAIL	SED FAIL	PARITY ERR FALL	PARITY ERR RISE			0X00
IRQ REQUEST 0	**0X05**	5	R/W	FIFO_WARN2	FIFO_WARN1	SPIFRMACK		DLL_WARN	DLL_LOCK	RETIME LOST	RETIME LOCK	0X00
IRQ REQUEST 1	**0X06**	6	R/W	PBIST DONE	AED PASS	AED FAIL	SED FAIL	PARITY ERR FALL	PARITY ERR RISE			0X00
FRAME PIN USAGE	**0X07**	7	R/W			PARUSAGE	FRMUSAGE			FRAME PIN USAGE<1:0>		0X00
	0X08	8	R/W									0X58
DATA CTRL 0	**0X0A**	10	R/W	DLL ENABLE	DUTY CORRECTION ENA			PHASE OFFSET <3:0>				0X40
DATA CTRL 1	**0X0B**	11	R/W	WARN CLEAR	LOCK DELAY DIVIDER	CONTROLLER CLOCK DIVIDER <1:0>						0X29
DATA CTRL 2	**0X0C**	12	R/W		DCO ENABLE							0X23
DATA CTRL 3	**0X0D**	13	R/W						DUTY CORRECTION BW <1:0>			0X04
DATA STAT 0	**0X0E**	14	R	DLL LOCK	DLL WARN	DLINE START WARN	DLINE END WARN		DCI ON		DLL RUNNING	~~
FIFO CTRL	**0X11**	17	R/W	SPIFRMREQ	SPIFRMACK	ENA PIN FRAMING					PHAZ REPORT ENA	0X00
FIFO OFFSET	**0X12**	18	R/W		RDPTROFF<2:0>				WRPTROFF<2:0>			0X04
FIFO CH0 THRM	**0X13**	19	R		PHZ0THRM<6:0>							~~
FIFO CH1 THRM	**0X14**	20	R		PHZ1THRM<6:0>							~~
FIFO CH2 THRM	**0X15**	21	R		PHZ2THRM<6:0>							~~
FIFO CH3 THRM	**0X16**	22	R		PHZ3THRM<6:0>							~~
FIFO 3.2 PHASE	**0X17**	23	R	FIFO WARN1	FIFO WARN2		3.2 FIFO PHASE<4:0>					~~
DATA MODE	**0X18**	24	R/W	DDR MODE	BINARY	FILT_SEL						0X00
DECODE CTRL	**0X19**	25	R/W								MIXMODE	0X00
SYNC	**0X1A**	26	R/W	INC LATENCY	DEC LATENCY		SYNC ENABLE	SYNC DONE	PHASE READBACK <2:0>			0X00
FSC_1	**0X20**	32	R/W	FULL SCALE CURRENT <7:0>								0X00
FSC_2	**0X21**	33	R/W						FSC BOOST	FULL SCALE CURRENT <9:8>		0X02
ANA_CNT1	**0X22**	34	R/W									0X00
ANA_CNT2	**0X23**	35	R/W									0X0C
CLK REG1	**0X30**	48	R/W		CROSS ENABLE	CROSS LOCATION<3:0>				DUTY_EN		0X00
RETIME CTRL 0	**0X33**	51	R/W	PHASE OFFSET <3:0>				CLEAR LOST				0X30
RETIME CTRL 1	**0X34**	52	R/W					PLL RESET				0X55
RETIME STAT 0	**0X35**	53	R	PLL LOCK	PLL LOST							~~
SED CONTROL	**0X50**	80	R/W	SED ENABLE	SED ERR CLEAR	AED ENABLE	0	0	AED PASS	AED FAIL	SED FAIL	0X00

REGISTER NAME	ADDRESS		TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEF
SED PATT/ERR R0L	**0X51**	81	R	SED PATTERN/ERROR RISE0<7:0>								0X00
SED PATT/ERR R0H	**0X52**	82	R			SED PATTERN/ERROR RISE0<13:8>						0X00
SED PATT/ERR R1L	**0X53**	83	R	SED PATTERN/ERROR RISE1<7:0>								0X00
SED PATT/ERR R1H	**0X54**	84	R			SED PATTERN/ERROR RISE1<13:8>						0X00
SED PATT/ERR F0L	**0X55**	85	R	SED PATTERN/ERROR FALL0<7:0>								0X00
SED PATT/ERR F0H	**0X56**	86	R			SED PATTERN/ERROR FALL0<13:8>						0X00
SED PATT/ERR F1L	**0X57**	87	R	SED PATTERN/ERROR FALL1<7:0>								0X00
SED PATT/ERR F1H	**0X58**	88	R			SED PATTERN/ERROR FALL1<13:8>						0X00
PARITY CONTROL	**0X5C**	92	R/W	PARITY ENABLE	PARITY EVEN	PARITY ERR CLEAR				PARERRFAL	PARERRRIS	0X00
PARITY ERR RISING	**0X5D**	93	R	PARITY ERROR RISING<7:0>								0X00
PARITY ERR FALLING	**0X5E**	94	R	PARITY ERROR FALLING<7:0>								0X00
DRIVE STRENGTH	**0X7C**	124	R/W	DCO DRIVE STRENGTH <1:0>								0X7C
PART ID	**0X7F**	127	R	PART ID <7:0>								0X03 OR 0X83

DEVICE CONFIGURATION REGISTER DESCRIPTION

SPI Communications Control Register

Address: 0x00, Reset: 0x81, Name: MODE

Table 16. Bit Descriptions for MODE

Bits	Bit Name	Description	RESET	Access
7	Three / Four Wire mode	0 = 4 wire Bidirectional 1 = 3 wire Unidirectional	1	RW
6	LSB / MSB Data Packing	0 = MSB first packing 1 = LSB first packing	0	RW
5	SoftReset	When 1, Performs a Software based reset	0	RW
4	Short/Long Addressing Mode	0 = 8 bit Preamble 1 = 16 bit Preamble	0	RW
3		Mirror Bit [4] for Safety	0	R
2		Mirror Bit [5] for Safety	0	R
1		Mirror Bit [6] for Safety	0	R
0		Mirror Bit [7] for Safety	1	R

Power Control Register

Address: 0x01, Reset: 0x48, Name: POWER DOWN

Table 17. Bit Descriptions for POWER DOWN

Bits	Bit Name	Description	Reset	Access
7	Bandgap Power down	1 = Bandgap is in power down mode	0	RW

Bits	Bit Name	Description	Reset	Access
		0 = Bandgap is active		
6	Iref Power down	1 = FSC is 0mA 0 = FSC is as programmed	1	RW
5	Bias Power down	1 = All Bias currents are off 0 = All Bias currents are on	0	RW
4	RESERVED	RESERVED	0	RW
3	RESERVED	RESERVED	1	RW
2	Clock Path Power down	1 = DAC Clock is powered down 0 = DAC Clock is active	0	RW
1	Retime RD	1 = PLL is in power down	0	RW
0	Data Receiver PD	1 = Data Receiver is powered down	0	RW

Interrupt Enable Register

Address: 0x03, Reset: 0x00, Name: IRQ_ENABLE0

Table 18. Bit Descriptions for IRQ_ENABLE0

Bits	Bit Name	Description	Reset	Access
7	FIFO Warn2 INT Enable	Enables the FIFO warning within 2 slots of overwrite interrupt	0	RW
6	FIFO Warn1 INT Enable	Enables the FIFO warning within 1 slots of overwrite interrupt	0	RW
5	SpiFrame Ack INT Enable	Enables the FIFO SPI based calibration acknowledgement from SpiFrmReq-->1	0	RW
4	RESERVED	RESERVED	0	R
3	DLL Warn INT Enable	Enables the DLL Warning flag that the DataReceiver is no longer locked	0	RW
2	DLL Lock INT Enable	Enables the DLL Warning flag that the DataReceiver is now locked	0	RW
1	Retimer Lost INT Enable	Enables the Retimer Lost Interrupt indication	0	RW
0	Retimer Lock INT Enable	Enables the Retimer Lock Interrupt indication	0	RW

Interrupt Flag Register

Address: 0x04, Reset: 0x00, Name: IRQ_ENABLE1

Table 19. Bit Descriptions for IRQ_ENABLE1

Bits	Bit Name	Description	Reset	Access
7	PRNG (Bist) Done INT Enable	Enables the BIST Done interrupt signalling that all vectors were processed	0	RW
6	AED Pass INT Enable	Enables the AED PASS interrupt reporting saying that 8 valid spamples captured	0	RW
5	AED Fail INT Enable	Enables the AED FAIL interrupt reporting that a mis-compare occurred	0	RW
4	SED Fail INT Enable	Enables the SED FAIL interrupt reporting that a mis-compare occurred	0	RW
3	Parity Falling Edge Enable	Enables the Parity Fail due to a Falling Edge based Parity detected error	0	RW
2	Parity Rising Edge Enable	Enables the Parity Fail due to a Rising Edge based Parity detected error	0	RW
1	RESERVED	RESERVED	0	R
0	RESERVED	RESERVED	0	R

Interrupt Flag Register

Address: 0x05, Reset: 0x00, Name: IRQ REQUEST 0

Table 20. Bit Descriptions for IRQ REQUEST 0

Bits	Bit Name	Description	Reset	Access
7	FIFO Warn2 INT Status	Indicates that the FIFO is within 2 slots of overwrite	0	R
6	FIFO Warn1 INT Status	Indicates that the FIFO is within 1 slots of overwrite	0	R
5	SPIFrame Ack INT Status	Indicates acknowledgement from SpiFrmReq-->1	0	R
4	RESERVED	RESERVED	0	R
3	DLL Warn INT Status	Indicates that the Data Receiver is close to coming unlocked and action is needed.	0	R
2	DLL Lock INT Status	Indicates that Data Receiver is now locked	0	R
1	Retimer Lost INT Status	Indicates that the Retimer is no longer locked	0	R
0	Retimer Lock INT Status	Indicates that the Retimer is now locked	0	R

Interrupt Select Register

Address: 0x06, Reset: 0x00, Name: IRQ REQUEST 1

Table 21. Bit Descriptions for IRQ REQUEST 1

Bits	Bit Name	Description	Reset	Access
7	PRNG (Bist) Done INT Status	Indicates that all BIST vectors were processed	0	RW
6	AED Pass INT Status	Indicates that the AED logic has captured 8 valid samples	0	RW
5	AED Fail INT Status	Indicates that the AED logic has detected a mis-compare	0	RW
4	SED Fail INT Status	Indicates the SED FAIL interrupt; reporting that a mis-compare occurred	0	RW
3	Parity Falling Edge Status	Indicates a Parity fault due to data captured on the Falling Edge	0	RW
2	Parity Rising Edge Status	Indicates a Parity fault due to data captured on the Rising Edge	0	RW
1	RESERVED	RESERVED	0	RW
0	RESERVED	RESERVED	0	RW

Interrupt Select Register

Address: 0x07, Reset: 0x00, Name: FRAME PIN USAGE

Table 22. Bit Descriptions for FRAME PIN USAGE

Bits	Bit Name	Description	Reset	Access
7	RESERVED	RESERVED	0	RW
6	RESERVED	RESERVED	0	RW
5	ParUsage	1 = Frame pin mode is Parity and Parity is Enabled	0	R
4	FrmUsage	1 = Frame pin mode is Frame and EnaPinFrm is enabled	0	R
3	RESERVED	RESERVED	0	R
2	RESERVED	RESERVED	0	R
[1:0]	FRAME PIN MODE	0 = No Effect 1 = Parity 2 = Frame 3 = RESERVED	0x0	RW

RESERVED_0 Register

Address: 0x08, Reset: 0x58, Name: RESERVED_0

Table 23. Bit Descriptions for RESERVED_0

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	RESERVED	0x58	R

Data Receiver Control 0 Register

Address: 0x0A, Reset: 0x40, Name: DATA CTRL 0

Table 24. Bit Descriptions for DATA CTRL 0

Bits	Bit Name	Description	Reset	Access
7	DLL Enable	1 = Enable DLL 0 = Disable DLL	0	RW
6	Duty Cycle Enable	1 = Enable Duty Cycle Correction 0 = Disable Duty Cycle Correction	1	RW
5	Manual Mode	1 = Use Manual Mode 0 = Use Automatic Mode	0	RW
4	Man Flip DCI	When Manual Mode is active, 1 = use inverted DCI to sample data 0 = use DCI to sample data	0	RW
[3:0]	Phase Offset	Locked Phase = 90 degrees + n*11.25 degrees, where n is the 4 bit signed magnitude number	0x0	RW

Data Receiver Control 1 Register

Address: 0x0B, Reset: 0x29, Name: DATA CTRL 1

Table 25. Bit Descriptions for DATA CTRL 1

Bits	Bit Name	Description	Reset	Access
7	Clear Warn	1 = Clear Data Receiver Warn Bit	0	RW
6	Lock Delay Divider	1 = long delay 0 = short delay	0	RW
[5:4]	Controller Clock Divider	Controller Clock Divider 00 = DCI/4 01 = DCI/16 10 = DCI/64 11 = DCI/512	0x2	RW
[3:0]	Delay Line Middle Set	Sets nominal delay line delay	0x9	RW

Data Receiver Control 2 Register

Address: 0x0C, Reset: 0x23, Name: DATA CTRL 2

Table 26. Bit Descriptions for DATA CTRL 2

Bits	Bit Name	Description	Reset	Access
7	RESERVED	RESERVED	0	RW
6	DCO Enable	1 = Enables DCO Output Driver	0	RW
[5:3]	Max Delay Set	Sets Max Delay Line Delay (larger = longer delay line)	0x23	RW

Data Receiver Control 3 Register

Address: 0x0D, Reset: 0x04, Name: DATA CTRL 3

Table 27. Bit Descriptions for DATA CTRL 3

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	RESERVED	0x00	R
[2:1]	Duty Correction BW Set	Controller Clock Divider 00 = Highest BW 01 = Higher BW 10 = Lower BW 11 = Lowest BW	0x2	RW
0	Duty Correction Sleep	1 = Duty Correction is temporarily disabled 0 = Duty Correction is enabled	0	RW

Data Receiver Status 0 Register

Address: 0x0E, Reset: 0x00, Name: DATA STAT 0

Table 28. Bit Descriptions for DATA STAT 0

Bits	Bit Name	Description	Reset	Access
7	DLL Lock	1 = DLL Lock	0	R
6	DLL Warning	1 = DLL Near Begin/End of Delay Line	0	R
5	DLL Start Warning	1 = DLL at Beginning of Delay Line	0	R
4	DLL End Warning	1 = DLL at End of Delay Line	0	R
3	DLL Correct Phase	1 = Data being sampled on correct phase. 0 = Data being sampled on incorrect phase.	0	R
2	DCI On	1 = User has provided a clock > 100 MHz	0	R
1	Lock Phase	0 = DLL has locked on positive half of DCI. 1 = DLL has locked on negative half of DCI.	0	R
0	DLL Running	1 = Closed Loop DLL attempting to lock, 0 = Delay fixed at middle of Delay Line	0	R

FIFO Control Register

Address: 0x11, Reset: 0x00, Name: FIFO CTRL

Table 29. Bit Descriptions for FIFO CTRL

Bits	Bit Name	Description	Reset	Access
7	SPIFrmReq	Requests a SPI based FIFO alignment (need to 0-->1-->0 with SPIFrmAck)	0	RW
6	SPIFrmAck	Acknowledge SPIFrmReq change (tracks SPIFrmReq setting)	0	RW
5	EnaPinFrm	When 1, enables Hardware Pin based FIFO Framing	0	RW
[4:1]	RESERVED	RESERVED	0x0	R
0	EnaPhazRep	When 1, enables FIFO Phase reporting	0	RW

FIFO Offset Register

Address: 0x12, Reset: 0x04, Name: FIFO OFFSET

Table 30. Bit Descriptions for FIFO OFFSET

Bits	Bit Name	Description	Reset	Access
7	RESERVED	RESERVED	0	R

Bits	Bit Name	Description	Reset	Access
[6:4]	RdPtrOff<2:0>	FIFO Read Pointer Offset (ONLY FOR LAB USE)	0x0	RW
3	RESERVED	RESERVED	0	R
[2:0]	WtPtrOff<2:0>	FIFO Write Pointer Offset	0x4	RW

FIFO Thermometer for Phase 0 Status Register

Address: 0x13, Reset: 0x00, Name: FIFO CH0 THRM

Table 31. Bit Descriptions for FIFO CH0 THRM

Bits	Bit Name	Description	Reset	Access
7	RESERVED		0	R
[6:0]	Phase 0 based FIFO Thermometer status	Phase 0 relative FIFO Phasing as: 0x0000000 .. 0x1111111 where 0x0000111 is considered the middle of the FIFO storage space	0x00	R

FIFO Thermometer for Phase 1 Status Register

Address: 0x14, Reset: 0x00, Name: FIFO CH1 THRM

Table 32. Bit Descriptions for FIFO CH1 THRM

Bits	Bit Name	Description	Reset	Access
7	RESERVED		0	R
[6:0]	Phase 1 based FIFO Thermometer status	Phase 1 relative FIFO Phasing as: 0x0000000 .. 0x1111111 where 0x0000111 is considered the middle of the FIFO storage space	0x00	R

FIFO Thermometer for Phase 2 Status Register

Address: 0x15, Reset: 0x00, Name: FIFO CH2 THRM

Table 33. Bit Descriptions for FIFO CH2 THRM

Bits	Bit Name	Description	Reset	Access
7	RESERVED	RESERVED	0	R
[6:0]	Phase 2 based FIFO Thermometer status	Phase 2 relative FIFO Phasing as: 0x0000000 .. 0x1111111 where 0x0000111 is considered the middle of the FIFO storage space	0x00	R

FIFO Thermometer for Phase 3 Status Register

Address: 0x16, Reset: 0x00, Name: FIFO CH3 THRM

Table 34. Bit Descriptions for FIFO CH3 THRM

Bits	Bit Name	Description	Reset	Access
7	RESERVED	RESERVED	0	R
[6:0]	Phase 3 based FIFO Thermometer status	Phase 3 relative FIFO Phasing as: 0x0000000 .. 0x1111111 where 0x0000111 is considered the middle of the FIFO storage space	0x00	R

FIFO Status Register

Address: 0x17, Reset: 0x00, Name: FIFO 3.2 PHASE

Table 35. Bit Descriptions for FIFO 3.2 PHASE

Bits	Bit Name	Description	Reset	Access
7	FIFO Warn 1	When 1, Write/Read pointers 1 cycle away from overwrite	0	R
6	FIFO Warn 2	When 1, Write/Read pointers 2 cycle away from overwrite	0	
5	0		0	
[4:0]	FIFO Phase as a Format 3.2 averaged value	Averaged FIFO Phasing represented as mmm.nn digits where - mmm represents the FIFO phasing as 0..7 where 3 or 4 is considered center - nn represents the phasing relative to the 4 internal clocks as 0..3 This data is not reliable if the Warn1 or Warn2 bit is set. Use the thermometer values for each FIFO's status instead.	0x00	

Data Mode Control Register

Address: 0x18, Reset: 0x00, Name: DATA MODE

Table 36. Bit Descriptions for DATA MODE

Bits	Bit Name	Description	Reset	Access
7	DDR Mode	0 = Bypass 2x interpolator filter 1 = Enable 2x interpolation filter	0	RW
6	Binary Select	Select input data format: 1=Unsigned 0=Signed	0	RW
5	FILT_SEL	2x interpolator filter select: 0 = 25 dB Out-of-Band (OOB) rejection 1 = 40 dB OOB rejection	0	R
[4:0]	RESERVED	RESERVED	0	R

Decoder Control (Program Thermometer Type) Register

Address: 0x19, Reset: 0x00, Name: DECODE CTRL

Table 37. Bit Descriptions for DECODE CTRL

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	RESERVED	0x00	R
0	Mix-mode Enable	1 = Mixmode 0 = Normal	0	RW

Sync Control Register

Address: 0x1A, Reset: 0x00, Name: SYNC

Table 38. Bit Descriptions for SYNC

Bits	Bit Name	Description	Reset	Access
7	Inc Latency	Increment delay by 1	0	RW
6	Dec Latency	Decrement delay by 1	0	RW
5	RESERVED	RESERVED	0	R
4	Sync Enable	1 = Enable multi-DAC sync function and pin 0 = Multi-DAC sync disabled	0	RW

Bits	Bit Name	Description	Reset	Access
3	Sync Done	1 = last increment or decrement request is complete	0	R
[2:0]	Phz Readback <2:0>	Readback of existing SYNC phase delay value	0	R

Full Scale Current Adjust (Lower) Register

Address: 0x20, Reset: 0x00, Name: FSC_1

Table 39. Bit Descriptions for FSC_1

Bits	Bit Name	Description	Reset	Access
7:0	DAC Gain Adj<7:0>	DAC full scale current(LSB part)	0x00	RW

Full Scale Current Adjust (Upper) Register

Address: 0x21 Reset: 0x02, Name: FSC_2

Table 40. Bit Descriptions for FSC_2

Bits	Bit Name	Description	Reset	Access
7	RESERVED	RESERVED	0	RW
[6:2]	RESERVED	RESERVED	0	R
1:0	DAC Gain Adj<9:8>	DAC full scale current (MSB part)	0x02	RW

Analog Control 1 Register

Address: 0x22, Reset: 0x00, Name: ANA_CNT1

Table 41. Bit Descriptions for ANA_CNT1

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	RESERVED	0x0	RW

Analog Control 2 Register

Address: 0x23, Reset: 0x0C, Name: ANA_CNT2

Table 42. Bit Descriptions for ANA_CNT2

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	RESERVED	0x0C	RW

Clock Control 1 Register

Address: 0x30, Reset: 0x00, Name: CLK REG1

Table 43. Bit Descriptions for CLK REG1

Bits	Bit Name	Description	Reset	Access
7	Force Cross Control	Force on Cross Control in case DAC On does not turn on	0	RW
6	Cross Enable	Enable Cross Control	0	RW
[5:2]	Cross Location	Adjust Cross Control Location (Sign-Mag)	0	RW
1	Duty Enable	Enable Duty Cycle Correction	0	RW
0	Select Internal	Select Internal Clock (DO NOT USE)	0	RW

Retime Control 0 Register

Address: 0x33, Reset: 0x30, Name: RETIME CTRL 0

Table 44. Bit Descriptions for RETIME CTRL 0

Bits	Bit Name	Description	Reset	Access
[7:4]	Phase Offset	4 Bit Sign Magnitude. PFD Phase = n*30 degrees. XOR = 90 + n*15 degrees.	0x3	RW
3	Clear Lost	Clear Lost Status Bit	0	
2	PLL Divider	1 = Divide by 4, 0 = Divide by 8	0	
[1:0]	Retime Mode	0 = Use PFD, 1 = Use XOR (0-180), 2 = XOR (180-360), 3 = Undefined	0x0	

Retime Control 1 Register

Address: 0x34, Reset: 0x55, Name: RETIME CTRL 1

Table 45. Bit Descriptions for RETIME CTRL 1

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	RESERVED	0x5	RW
3	Reset PLL	1 = Reset the DAC clock PLL 0 = Normal operation for DAC clock PLL	0	RW
[2:0]	RESERVED	RESERVED	0x5	RW

Retime Status 0 Register

Address: 0x35, Reset: 0x00, Name: RETIME STAT 0

Table 46. Bit Descriptions for RETIME STAT 0

Bits	Bit Name	Description	Reset	Access
7	PLL Lock	1 = Retimer PLL Locked	0	R
6	PLL Lost	1 = Retimer PLL Lost (Can be sticky)	0	R
[5:4]	RESERVED	RESERVED	0x0	R
[3:0]	ADC Readback	Control Voltage Readback	0x0	R

Sample Error Detection (SED) Control Register

Address: 0x50, Reset: 0x00, Name: NCO_PHASE_OFFSET1

Table 47. Bit Descriptions for NCO_PHASE_OFFSET1

Bits	Bit Name	Description	Reset	Access
7	SED Enable	Set to 1 to Enable the SED Compare Logic	0	RW
6	SED Error Clear	When 1, clears all SED reported error bits below	0	RW
5	AED Enable	When 1, enables the AED function { SED with auto clear after 8 passing sets }	0	RW
4	RESERVED	RESERVED	0	R
3	RESERVED	RESERVED	0	R
2	AED PASS	When AED=1, Signals 8 true compare cycles	0	RW
1	AED FAIL	When AED=1, Signals a mis-compare	0	R
0	SED FAIL	Signals that an SED mis-compare occurred (With SED or AED enabled)	0	R

Sample Error Detection (SED) Channel 0 Rising Edge Status Low Register

Address: 0x51, Reset: 0x00, Name: SED PATT/ERR R0L

Table 48. Bit Descriptions for SED PATT/ERR R0L

Bits	Bit Name	Description	Reset	Access
[7:0]	SED Channel 0 Rising Edge Low Part Error Bits	SED Ch0 Rising Edge Error Bits <7:0>	0x00	R

Sample Error Detection (SED) Channel 0 Rising Edge Status High Register

Address: 0x52, Reset: 0x000, Name: SED PATT/ERR R0H

Table 49. Bit Descriptions for SED PATT/ERR R0H

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	RESERVED	0x0	R
[5:0]	SED Channel 0 Rising Edge High Part Error Bits	SED Ch0 Rising Edge Error Bits <13:8>	0x00	R

Sample Error Detection (SED) Channel1 Rising Edge Status Low Register

Address: 0x53, Reset: 0x00, Name: SED PATT/ERR R1L

Table 50. Bit Descriptions for SED PATT/ERR R1L

Bits	Bit Name	Description	Reset	Access
[7:0]	SED Channel 1 Rising Edge Low Part Error Bits	SED Ch1 Rising Edge Error Bits <7:0>	0x00	R

Sample Error Detection (SED) Channel1 Rising Edge Status High Register

Address: 0x54, Reset: 0x00, Name: SED PATT/ERR R1H

Table 51. Bit Descriptions for SED PATT/ERR R1H

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	RESERVED	0x0	R
[5:0]	SED Channel 1 Rising Edge High Part Error Bits	SED Ch1 Rising Edge Error Bits <13:8>	0x00	R

Sample Error Detection (SED) Channel 0 Falling Edge Status Low Register

Address: 0x55, Reset: 0x00, Name: SED PATT/ERR F0L

Table 52. Bit Descriptions for SED PATT/ERR F0L

Bits	Bit Name	Description	Reset	Access
[7:0]	SED Channel 0 Rising Edge Low Part Error Bits	SED Ch0 Rising Edge Error Bits <7:0>	0x00	R

Sample Error Detection (SED) Channel 0 Falling Edge Status High Register

Address: 0x56, Reset: 0x000, Name: SED PATT/ERR F0H

Table 53. Bit Descriptions for SED PATT/ERR F0H

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	RESERVED	0x0	R
[5:0]	SED Channel 0 Rising Edge High Part Error Bits	SED Ch0 Rising Edge Error Bits <13:8>	0x00	R

Sample Error Detection (SED) Channel1 Falling Edge Status Low Register

Address: 0x57, Reset: 0x00, Name: SED PATT/ERR F1L

Table 54. Bit Descriptions for SED PATT/ERR F1L

Bits	Bit Name	Description	Reset	Access
[7:0]	SED Channel 1 Rising Edge Low Part Error Bits	SED Ch1 Rising Edge Error Bits <7:0>	0x00	R

Sample Error Detection (SED) Channel1 Falling Edge Status High Register

Address: 0x58, Reset: 0x00, Name: SED PATT/ERR F1H

Table 55. Bit Descriptions for SED PATT/ERR F1H

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	RESERVED	0x0	R
[5:0]	SED Channel 1 Rising Edge High Part Error Bits	SED Ch1 Rising Edge Error Bits <13:8>	0x00	R

Parity Control Register

Address: 0x5C, Reset: 0x00, Name: PARITY CONTROL

Table 56. Bit Descriptions for PARITY CONTROL

Bits	Bit Name	Description	Reset	Access
7	Parity Enable	Set to 1 to Enable Parity	0x00	RW
6	Parity Even	0 – Odd Parity 1 – Even Parity	0	RW
5	Parity Error Clear	Set to 1 to clear Parity error counters.	0	RW
[4:2]	RESERVED	RESERVED	0x0	R
1	Parity Error Falling Edge	When 1, signals a Falling Edge Parity Error was detected	0	R
0	Parity Error Rising Edge	When 1, signals a Rising Edge Parity Error was detected	0	R

Parity Rising Edge Count Register

Address: 0x5D, Reset: 0x00, Name: PARITY ERR RISING

Table 57. Bit Descriptions for PARITY ERR RISING

Bits	Bit Name	Description	Reset	Access
[7:0]	Parity Rising Edge Error Count	Number of Rising Edge Based errors detected clipped to 256	0x00	R

Parity Falling Edge Count Register

Address: 0x5E, Reset: 0x00, Name: PARITY ERR FALLING

Table 58. Bit Descriptions for PARITY ERR FALLING

Bits	Bit Name	Description	Reset	Access
[7:0]	Parity Falling Edge Error Count	Number of Falling Edge Based errors detected clipped to 256	0x00	R

Drive Strength Register

Address: 0x7C, Reset: 0x7C, Name: DRIVE STRENGTH

Table 59. Bit Descriptions for DRIVE STRENGTH

Bits	Bit Name	Description	Reset	Access
[7:6]	DCO Drive Strength	Sets DCO drive strength: 00 = 2 mA 01 = 2.8 mA (default) 10 = 3.4 mA 11 = 4 mA	0x1	R/W
[5:0]	RESERVED	RESERVED	0x3C	R/W

Part ID Register

Address: 0x7F, Reset: 0x03 or 0x83, Name: PART ID

Table 60. Bit Descriptions for PART ID

Bits	Bit Name	Description	Reset	Access
[7:0]	Part ID	Version Information: 0x03 – AD9129 (14-bit version) 0x83 – AD9119 (11-bit version)	0x03 or 0x83	R